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Greetings from Rtn. Ponnuchamy
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It is important that our researchers in the fields of engineering and technology publish their research readily on a regular basis. This will help transfer of knowledge and skills from teaching and research institutions to manufacturing companies. Ultimately such transfers will help common people who would enjoy the benefits of such transfers in products and services extended to them. I wish great success to the journal of **Engineering & Technology in India** www.engineeringandtechnologyinindia.com.

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PTMAC BASED ON RAZOR FOR ENERGY REDUCTION IN DSP

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Abstract

The power optimization is achievable by dynamic voltage scaling using the fault tolerant technique by improving the accuracy and/or timing performance against power. Energy improvements have a strong dependency on the delay distribution of the circuit and the characteristics of the input signal. The fault tolerant technique is implemented using Razor approach. The target power is also obtained by using the programmable truncated multiplier (PTMAC) at the expense of degradation of the output signal to noise ratio. In the DSP architecture, the combination of PTMAC and fault tolerant technique is used to reduce the supply voltage below the critical level. Truncated multiplication timing modulation properties are analysed and demonstrated using Xilinx 12.1. Finally the two techniques upgrade the energy saving beyond that expected in the DSP architecture.

Key words: PTMAC, DSP, Razor, energy reduction.

INTRODUCTION

Less power, area with high speed is the main theme in the VLSI based circuit design. Several techniques exist to reduce the energy consumption.

Voltage scaling is an effective technique to reduce the energy consumption in CMOS integrated circuits. The (DSP) digital signal processing system may possibly leverage unconventional voltage overscaling (VOS) to reduce energy consumption while maintaining satisfactory signal processing performance. Scaling the supply

voltage by a factor of K results in reduction in the dominating dynamic power consumption by a factor of K^2 and yields static power benefits [1].

In conventional practice, voltage scaling is lower bounded by $V_{dd\text{-}crit}$ (critical supply voltage) under which critical path delay equals the target clock period, voltage overscaling (VOS) (i.e.), overscaling the supply voltage below $V_{dd\text{-}crit}$. Digital signal processing systems by applying unconventional voltage overscaling levels to further improve the energy consumption levels while maintaining signal processing performance. The major disadvantage of VOS is the latches or flip-flop on the critical path need a long execution time [3]-[5].

Fault tolerant is a property that enables a system to continue operating properly in the event of failure. This technique can be used to achieve power saving. It is dependent on process voltage temperature (PVT) and the circuit physical design.

The ultimate aim is to design a multiplier of which possess less area usage and power that is possible with the truncated multiplier [6]-[12]. The PTM describes a full precision multiplier in which the elements of the partial product can be disabled a column wise manner through an external control word. This provides reduction in the dynamic power consumption. The advantages include dynamic power reduction and Flexibility in accuracy selection.

Manuel de la Guia Solaz and Richard Conway proposed a novel voltage management technique for dynamic voltage scaled (DVS) processor, based on it situ error detection and correction, called Razor [4]. In this technique, we use a delay-error tolerant flip-flop on the critical path to scale the supply voltage.

The PTMAC and the fault tolerant techniques are applied to a custom-designed fixed point multiply and accumulate (MAC) in the DSP structure.

The rest of this paper is organised as follows. The voltage scaling, fault tolerant and truncated multiplication concept is dealt with in section II. Section III briefly explains the programmable truncated multiply and accumulate (PTMAC) architecture. The combination of the PTMAC and the fault tolerance using Razor technique is analysed in section IV. Simulation result for power and energy reductions is reported in section V. Finally in section VI conclusion and scope for future work on this paper are presented.

II BACKGROUND

A. Voltage Scaling Beyond $V_{dd\text{-}crit}$

Dynamic power consumption is the dominating component in many arithmetic unit circuits because of the high toggling profile of such structures. The switching component of the energy consumed by a digital gate is defined as $P\text{avg} = \alpha 0 \rightarrow 1 CLV2$ dd $f$clk in [13], where $\alpha 0 \rightarrow 1$ is defined as the average number of times in each clock cycle (at a frequency $f$clk) that a node with capacitance CL makes a power consuming transition. Reducing the supply voltage by a factor of K results in a quadratic improvement in the power consumption rate of CMOS logic.

Scaling of Vdd results in timing penalties which increase as Vdd approaches the threshold voltages of the devices [14]. Relationship between the circuit delay (τd) and the supply voltage Vdd is given by $\tau d = CLV\text{dd}/\beta(V\text{dd} - Vt)\alpha$, where CL is the load capacitance, β is the gate transconductance, Vt is the device threshold voltage, and α is the velocity saturation index. We refer to the critical supply voltage of a given architecture Vdd−crit, as the minimum supply voltage where timing on the critical path is met for any expected PVT variations.

Scaling the supply voltage to $V\text{dd} = K \cdot V\text{dd}-\text{crit}$, where $0 < K < 1$ is referred to as VOS; although this technique results in further energy reductions almost proportional to $K2$, scaling Vdd below the critical supply voltage results in critical

timing failures for certain input combinations under certain PVT conditions. This is impractical for use with designs that do not apply fault tolerant schemes.

III TRUNCATED MULTIPLICATION

Multipliers have become inevitable with the advancement of communication. In order to enable the implementation of complex algorithms in DSP architectures the advancing VLSI play a significant role. A truncated multiplier is an n × n multiplier with n bits output. Since in a truncated multiplier the n less significant bits of the full-width product are discarded, some of the partial products are removed and replaced by a suitable compensation function, to trade- off accuracy with hardware cost. As more columns are eliminated, the area and power consumption of the arithmetic unit are significantly reduced, and in many cases the delay also decreases. Truncated Multiplier has the advantage of reducing power consumption in the DSP systems. It is most commonly used in systems where least significant part of partial product can be skipped or disabled which leads to low power consumption, area and timing. Here the partial product is split into two sections namely the Least Significant Part (LSP) and Most Significant Part (MSP). The LSP is disabled or avoided to get the truncated output.

Truncated multiplication has been widely studied as a means of achieving both power and area improvements in the field of arithmetic circuit design, at the expense of signal degradation. As the truncated multipliers are smaller than full-precision ones, they not only achieve improvements in power consumption and area, but result in different timing distributions. The existence of synergic benefits derived from the combination of truncated multiplication and VOS using a fault tolerance strategy is presented in this brief where both techniques are applied to a custom-designed fixed point multiply and accumulate (MAC) structure.

IV PTMAC-A FLEXIBLE LOW-POWER DSP WITH PTM

To extend the usage of PTM to general DSP architectures, the PTMAC was introduced and analyzed in [12] and [19]. PTMAC, designed as a vehicle to exercise PTM in low-power biomedical applications with a need for modest DSP such as ECG filtering or fall detection, will be utilized in this brief as a platform to combine the benefits of programmable truncation and fault tolerance.

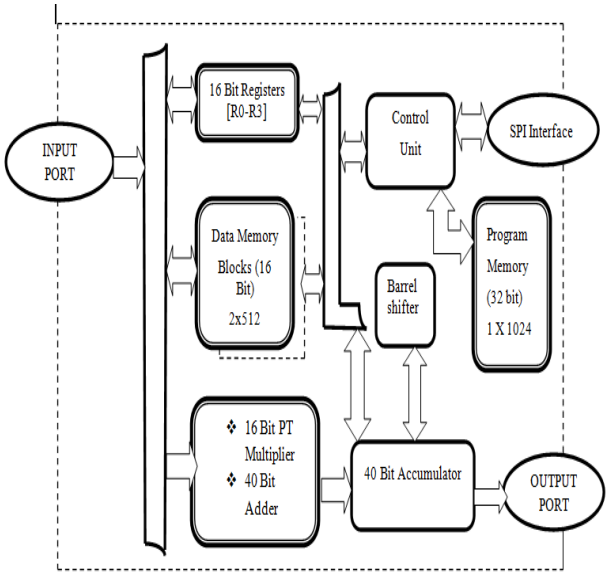

Fig.1. PTMAC top level diagram.

The proposed DSP, as depicted in Fig. 1, includes a control unit operating in a five-stage pipeline, program and memory blocks in a multibus Harvard configuration, some I/O connectivity and an arithmetic unit consisting of a MAC structure with a 16-bit PTM, a 40-bit accumulator, and a 40-bit barrel shifter for scaling and rotating the accumulated value.

The following gives the description of the main components of the DSP architecture.

1) Control unit: The control unit is a simple 5 stage pipeline which fetches and decodes the instruction also controls the data flow ,controls the ALU operations. The main aim of the design of the control unit is to reduce the power consumption of the internal blocks other than the arithmetic block. it allows the access of two data memory blocks and the program memory block during the instruction read operation.

2) Custom Instruction Set: A custom instruction set is implemented for the DSP so as to maximize the utilization of the ALU. This will help in optimizing the power reductions Offered by the programmable truncated multiplier. All the Instructions designed are 32 bits wide. The set of instructions include

- **Arithmetic and logic instructions:** The arithmetic instruction include addition operation, subtraction, multiplication with and without truncation and also other operations such as multiply and accumulate operation, shifting and rotation of the accumulator output also squaring of the accumulated value. All the arithmetic instructions utilize the arithmetic unit effectively. A logic instruction performs all the logic operations.
- **Flow control instructions:** The flow control instructions include instructions for jump operation, loop operations. Table III presents a list of such instructions.
- **Dataflow instructions:** It includes instructions for storing and loading data to and from different memory blocks.

3) Memory blocks: The memory blocks include two data memory blocks a program memory block. Each data memory is of size 512 x16 bits and the program memory is of size 1024x32 bit. The data memory is used to store and load data, .and program memory is used to store the instructions. it is possible to access all the three memory blocks in a single clock cycle.

4) Arithmetic and logic unit: The ALU contains the 16 bit programmable truncated multiplier, a 40 bit carry select adder a 40 bit barrel shifter/rotator and a 40 bit accumulator. The ALU has a multiply and accumulate structure. . A block diagram of the Arithmetic Unit is displayed in Fig. The arithmetic unit consists of

- **PTM:** The PTM is designed to operate as a standard 16x16 bit multiplier that enables a programmable truncation. For that it includes an extra control input for enabling and disabling the columns in the partial product matrix. Thus the

extra control input “truncation control” is used to control the truncation level of the multiplier.

- **Barrel shifter:** A 40 bit barrel shifter/rotator is used for shifting as well as rotating the accumulated output. The shifter performs left shifting, left rotation, right shifting and right rotation on the 40 bit accumulator output.

- **Accumulator:** A 40 -bit accumulator stores the final result of the arithmetic operations. It is constructed from D flipflops.

- **Carry Select Adder:** A 40- bit carry select adder is used for addition as well as subtraction operations. The carry select adder is a simple but high speed adder. The logic unit performs all logic operations on the two input data.

V RAZOR IMPLEMENTATION

To achieve the fault tolerance, the accumulator unit of the PTMAC was replaced by a fault tolerant version named Razor Accumulator where the original flip-flops were substituted by a version of the Razor registers presented in [3] and [20].

In order to detect an error at the circuit level, each flip-flop is augmented by a shadow flip-flop which is clocked by a delayed clock. If the combinational logic met the setup time of the main flip-flop, then the main and delayed flip-flop will latch the same value. In this case, the error signal remains low. If the setup time of the main flip-flop is not met, then the main flip-flop will latch a value that is different from the shadow flip-flop.

The proposed augmented cells were designed and stored as library cells for post synthesis insertion. Such a cell follows the original implementation Razor implementation, replacing the shadow latch within the Razor registers with a shadow-flip-flop to avoid synthesis issues. The metastability detector required in Razor implementations was modelled as the delay of an inverter added as a constraint to the hold time of the Razor accumulator. In this way, all timing violations potentially

causing metastability are then detected as timing errors, providing a lower bound for the performance of Razor.

The Razor technique was implemented using NI multisim suite 12.0 software.

VI RESULTS

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	0	46560	0.0
Signals	0.000	178	---	---
IOs	0.000	66	240	27.5
DSPs	0.000	2	288	0.7
Leakage	0.712			
Total	0.712			

Fig .2. Power value of normal multiplier

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	61	46560	0.1
Signals	0.000	109	---	---
IOs	0.000	67	240	27.9
Leakage	0.712			
Total	0.712			

Fig .3. Power value of PT Multiplier

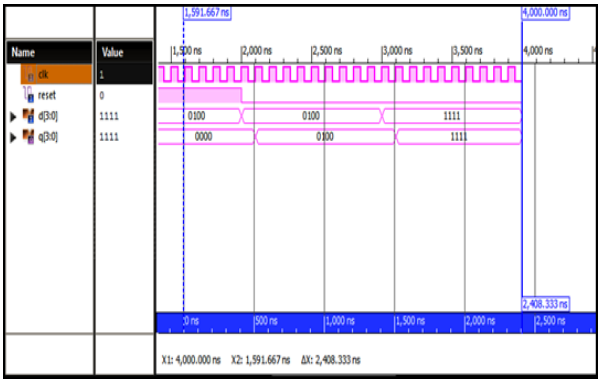

Fig .4. Simulation result of 16 bit Register

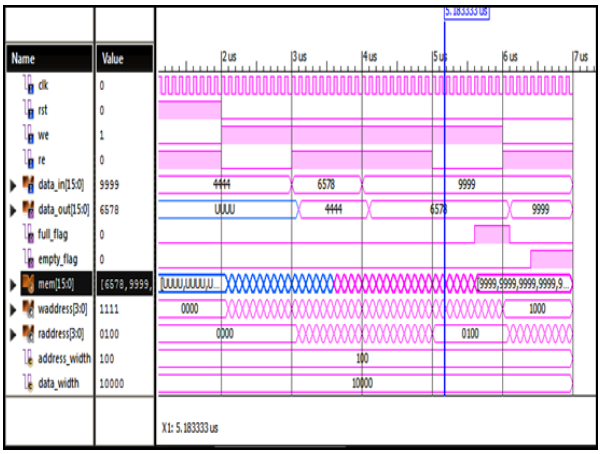

Fig .5. Simulation result of data memory

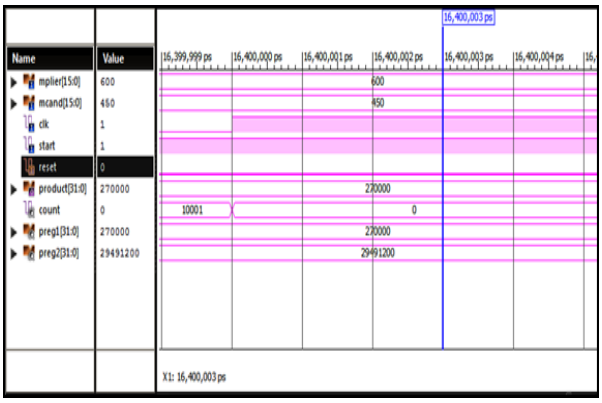

Fig .6. Simulation result of 16 bit PT multiplier

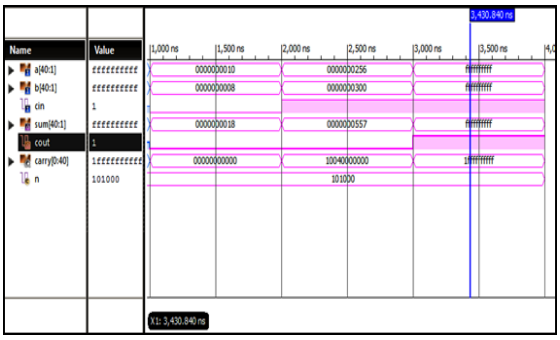

Fig .7. Simulation result of 40 bit Adder

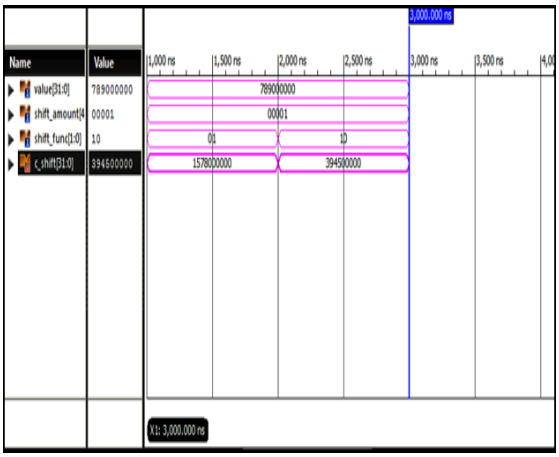

Fig .8. Simulation result of Barrel Shifter

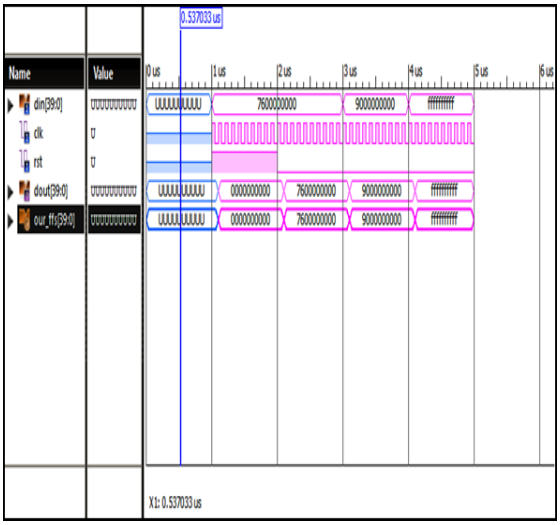

Fig .9. Simulation result of Accumulator

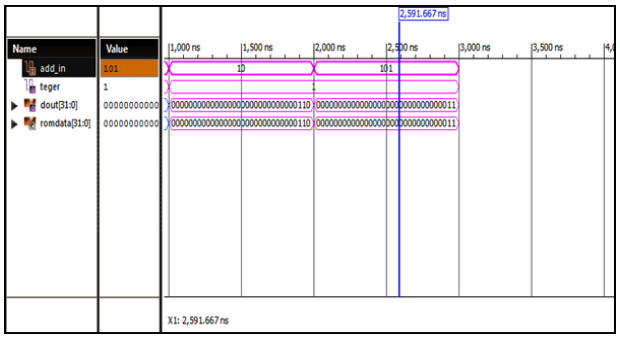

Fig .10. Simulation result of Program memory

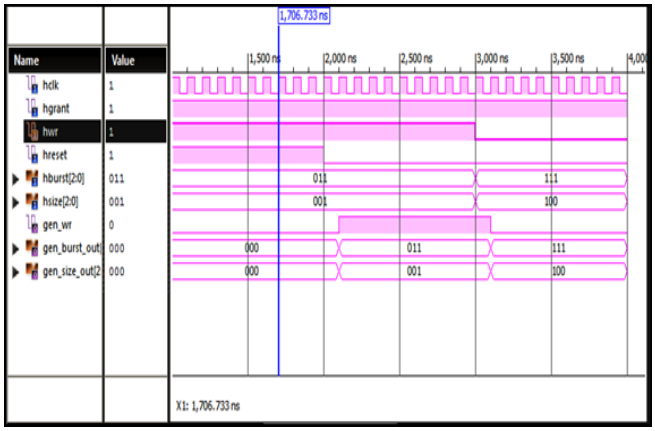

Fig .11. Simulation result of Control Unit

A. COMPARISION

MULTIPLIER	POWER (in %)
Normal Multiplier	28.2

SUPPLY VOLTAGE(V)	PTMAC BLOCK	RAZOR TECHNIQUE
20 V	800 (pW)	425 (pW)
17 V	578 (pW)	314 (pW)
12 V	288 (pW)	169 (pW)
10 V	200 (pW)	125 (pW)
7 V	98 (pW)	74 (pW)

Table .1. Power range of Normal and PT multiplier

PT Multiplier	28.0

TECHNIQUE	POWER (in %)
PTMAC BLOCK	81.9
MODIFICATION IN SP INTERFACE	81.8

Table .2. Overall power value

Table .3. Power of PT and Razor technique

VII CONCLUSION

Fault tolerance was provided by implementing a conservative approach to the Razor I technique, and achieved energy reductions over the original DSP implementation by enabling the reduction of V_{dd} beyond the original critical supply level. Truncated multiplication was achieved by implementing a PTM, and resulted in energy savings of the full design. Energy reductions achieved by fault tolerant techniques are limited by the overheads required to provide error resilience and the amount of operations that need correction, therefore, they are highly influenced by the delay distribution and maximum value of the system critical paths. The truncated multiplication is achieved by interfacing them effectively with respect to the conditions after checking and monitoring than the previous method. The use of Razor on a PTMAC structure has been tested at a post synthesis simulation level to study the effect and interactions of both energy reducing techniques on a previously tested DSP design. The timing and power effects of VOS with error correction and the application of programmable truncated multiplication resulted in significant power reductions. The power consumption of Razor on a PTMAC structure is also implemented in Multisim software. Thus, we have analyzed and compared the performance results better than the conventional approach in terms of area, power and speed.

In the future work, delay-modulation properties of truncated multiplication and BIST using testable circuits can be exploited to improve the energy consumption of fault tolerant DSP architectures where multipliers are involved in the critical path of the circuit.

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Design of Water Analyzer Using Pulse Voltametry

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ABSTRACT

This work proposes the development of a new approach for water sample authentication, in real life, using a pulse-voltametry-method-based electronic tongue instrumentation system. The system is developed as a parallel combination of several neural network classifiers; each dedicated to authenticate a specific category of water sample, and can be extended for more categories of water sample authentication. The system employs a slant let-transform (ST)-based feature extraction module and two popular variants of neural networks for classification. The proposed system hybridizes ST with two variants of back propagation-neural-network-based binary classifiers to develop an automated authentication tool. ST is regarded as an improved version of orthogonal discrete wavelet transform that can provide improved time localization with simultaneous achievement of shorter supports for the filters. This proposed system, implemented in a laboratory environment for various water samples available in India, showed encouraging average authentication percentage accuracy, on the order of over 80% for most water categories and even producing accuracy results exceeding 90%, for several categories.

Key words: Design water analyzer, pulse voltametry, electronic tongue

1 INTRODUCTION

Electronic tongues have been applied to many different fields in the last decades. However, it is in the food quality control and safety where the applicability of these biomimetic systems has been explored more. These electronic tongue systems are mainly optimized for the analysis of water samples. This technique is highly reliable, but it requires several experimental steps (sample preparation, DNA extraction, micro satellite amplification and gel electrophoresis) and skilled personnel to carry out. Recently, a review has covered the research done in the field of electronic and bioelectronics' tongues for the analysis of water samples. However, one special point that was not covered enough in this review is the data fusion of various measurement techniques

(potentiometry, amperometry, conductance, spectrophotometry, gas sensing). These systems are called hybrid electronic tongues because they merge variables of different nature.

The E-tongue device is built with a potentiostat interfaced with an intelligent .A potentiostat is used for electrochemical characterization of redox active species and in evaluating thermodynamic and kinetic parameters of electron transfer events. A potentiostat is an electronic instrument that is capable of imposing electrical potential waveforms across a working electrode relative to a reference electrode. It also measures the resultant current through the cell at the third electrode.

In operation, the potentiostat is commonly interfaced to a three-electrode setup containing reference electrode, working electrode, and counter electrode. The reference electrode establishes a constant reference potential in the electrochemical cell, against which the working electrode potential may be determined with relatively high precision. Minimal current is drawn through the reference electrode because its current signal is made input to a very high impedance electrometer, thus ensuring the constant potential condition. The working electrode is the surface at which the electron transfer of interest occurs.

2 RELATED WORKS

Characterization of liquid substances and compounds has been often inexact due to inhomogeniety of the species in the liquid, fluctuations in the interaction with the sensor, and the difficulty in interpretation based on quantitative or qualitative analysis. The conventional sensor systems that are capable of overcoming these problems often become bulky and expensive. in recent years, multisensory systems have been developed, called electronic tongue (popularly known as e-tongue) systems, which are capable of sensing the characteristics of wet chemical by a special data Acquisition method called voltametric method. Time series signals and the corresponding raw data, representing the measurement from a multisensory system, can give rise to large Matrices, sometimes with several thousands of entries, and can be analyzed using multivariate statistical methods (e.g., principle component analysis (PCA). In most cases, these time series raw data contain noise due to drift, which may yield misinterpretation about qualitative discrimination. This is because the PCA method can only reduce the dimensionality of the time series raw data but cannot eliminate the effect of noise and drift. it is recently reported that wavelet transform (wt)-

based methods can also be advantageously used in these problems . They can compress, Denise, or smooth large complicated signals used in many fields, e.g., in electrochemistry. Several e-tongue systems have so far been developed for quality assessment of water and other beverages and also, several electronic nose systems have been developed for water and beverage quality assessment and odor or flavor classification. In, a fuzzy clustering technique has been developed to determine prototypes for good and bad quality from a set of training data, acquired from the pulse voltametry technique. This method has been applied for water and baby food quality assessment. In water quality assessment, although they recorded good results for tap water and river water, their results were not that encouraging for boiled river water and mixtures.

Another e-tongue system where two fuzzy adaptive resonance theory map (art map)-based classifiers were developed to discriminate between different waters, and they could achieve classification accuracy rates of 91.1% and 93.3%, respectively. In, a voltametric-technique-based e-tongue system was developed for qualitative analysis of water, where discrete cosine- transform-based dimensionality reduction techniques were investigated. In, another pulse-voltametry-based E-Tongue system was developed for the assessment of water using the PCA technique. However, to the best of our knowledge and belief, the proposed work in this literature is the first work to utilize an e-tongue system for liquid authentication (in our case, the liquids considered are different categories of water). In the present research work, we have utilized ST to extract features from the no stationary signals, acquired as the output from the e-tongue instrumentation system for each water sample, treated as a finite-length data signal. For each such signal, we have extracted relevant ST filter coefficients, and then, we have implemented a supervised-neural-network-based classifier as a six-input–one-output system. The output of the neural network- based binary classifier belongs to either of the two labels: one corresponding to the correct water category, implying that the sample is authenticated, and the other corresponding to the incorrect water category, implying that the sample is not authenticated. Hence, for authenticating *m* category of water samples, *m* such artificial-neural-network (ANN)-based binary authentication modules are developed, which are implemented in parallel.

Both supervised and unsupervised neural networks have been successfully employed, over the years, for classification, pattern recognition, function approximation, and estimation purposes [13]. in our present work, we employed two types of back propagation neural networks (BPNNS), one utilizing levenberg–marquardt learning (called henceforth BPNNLM) and the other utilizing

resilient back propagation learning (called henceforth BPNN-RP). The performances of these systems are evaluated in real life by implementing an e-tongue based instrumentation system with pulse voltametry method of experimentation, acquiring signals for samples tested from eight water categories and then building the water sample authentication system, utilizing ST-based feature extraction coupled with the neural-network-based authenticator. For each category of water, output signals were captured for two types of working electrodes (Ag and pt) in the e-tongue system, and the performance of the authentication system developed was tested for signals acquired from experimentations carried out with both sets of working electrodes. The proposed system showed encouraging authentication percent accuracy results for all categories of water samples, for both sets of working electrodes used.

3 METHODOLOGY

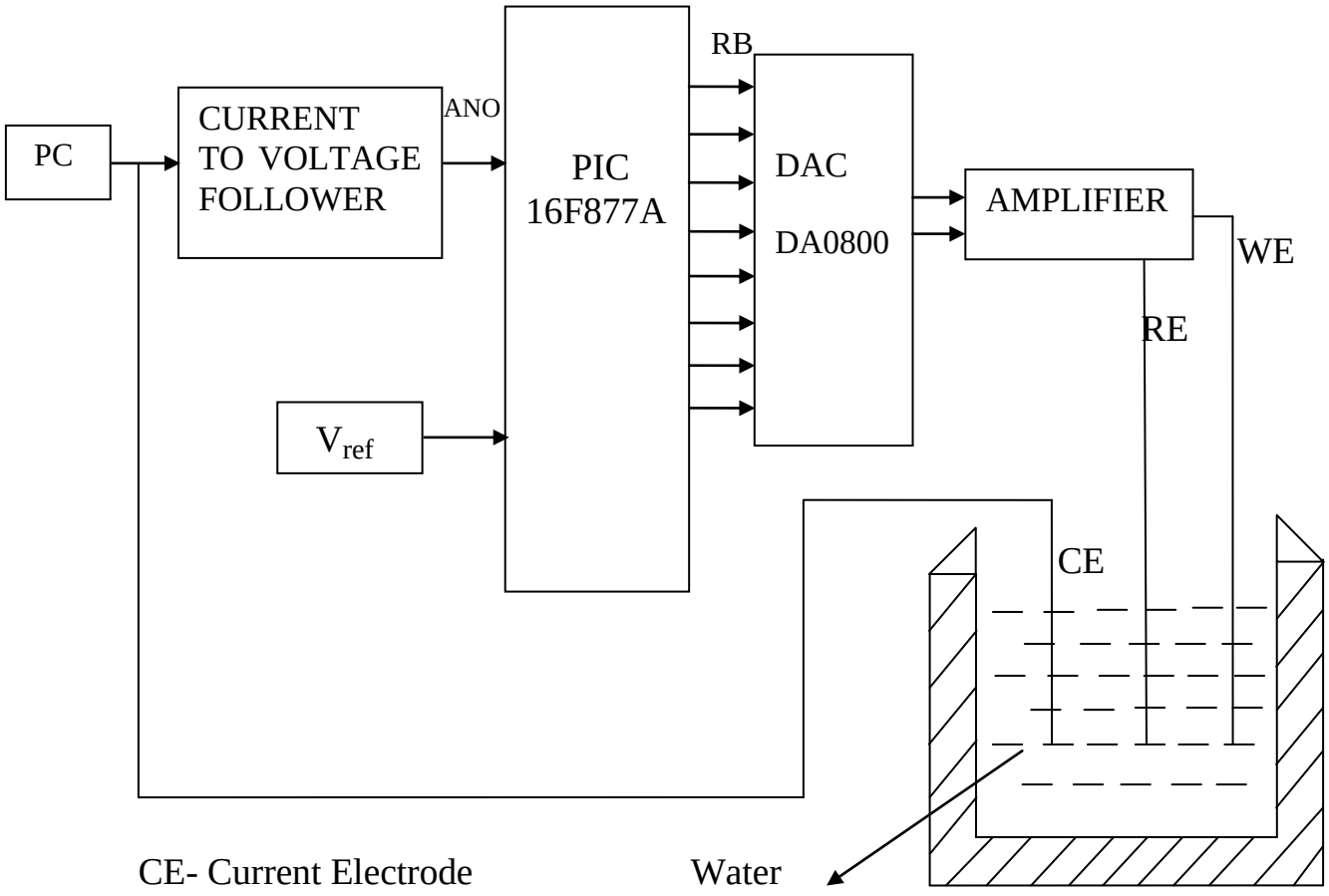
The E-tongue device is built with a potentiostat interfaced with an intelligent system (e.g., PC, microcontroller-based system, etc.). A potentiostat is used for electrochemical characterization of redox active species and in evaluating thermodynamic and kinetic parameters of electron transfer events. A potentiostat is an electronic instrument that is capable of imposing electrical potential waveforms across a working electrode relative to a reference electrode. It also measures the resultant current through the cell at the third electrode [2]. Potentiostat are widely used in electro analytical techniques to identify, quantify, and characterize redox active species, including inorganic, organic, and biochemical species.

In operation, the potentiostat is commonly interfaced to a three-electrode setup containing reference electrode, working electrode, and counter electrode. The reference electrode establishes a constant reference potential in the electrochemical cell, against which the working electrode potential may be determined with relatively high precision. Minimal current is drawn through the reference electrode because its current signal is made input to a very high impedance electrometer, thus ensuring the constant potential condition. The working electrode is the surface at which the electron transfer of interest occurs. Popular choices for the working electrode material include platinum, gold, silver, iridium, etc. Current arising from the electron transfer events at the working electrode is measured at the counter electrode, and therefore, this electrode must be geometrically larger than the working electrode so that it does not limit the current density at the working electrode.

The underlying technique in E-Tongue is known as electro analytical method. Commonly used methods are the following:

1) Voltametry and 2) potentiometry.

There are also other methods which can be followed, e.g., conductometry and spectrophotometry. Among these, voltametry appears to have several advantages. The technique has been extensively used in analytical chemistry due to features such as its very high sensitivity, versatility, simplicity, and robustness. There are different types of voltametry methods employed, e.g., cyclic, stripping, and pulse voltametry methods. Depending on the technique employed, various kinds of information can be obtained from the analytic. Using voltametry, the response can be obtained in less than 30 s, while potentiometry requires several minutes to complete a measurement sequence. The time aspect is important in a quality monitoring system since quality change can occur fast, and a quick response is therefore required. In E-Tongue, having a three-electrode configuration, potential is applied at the working electrode while the resulting current between the working electrode and the counter electrode is measured.



WE-Working Electrode

RE-Reference Electrode

Fig 1 – Functional blocks of water analyzer

In the pulse voltametry method, the input waveform is formed by potential pulses of varying amplitudes with a base potential in between. Different amplitudes are used to increase the sensitivity and improve the discrimination between samples. The reason for improvement in the sensitivity is that all substances that are electrochemically active below the applied potential will add to the measured current. The response current from an input pulse is composed of two currents: the Faradic current *IF* and the charging current *IC*.

3.1 BACK PROPAGATION-LEARNING-BASED NEURAL NETWORK AUTHENTICATOR

BPNNs are popularly employed for supervised learning to determine complex nonlinear multidimensional mathematical mapping. Over the years, different popular improved variations of BPNN have been proposed to specifically address several important issues, namely, reduction of convergence time, avoiding local minima and arriving at the global minimum, ease of computational burden, reduced memory requirement, etc.

In this paper, we consider two popular variants of BPNN, namely, BPNN-LM and BPNN-RP. For our problem under consideration, i.e., the development of an *M*-category authentication system, we have developed *M* such binary classifiers where each classifier can authenticate a specific category of water samples. The system so developed is generic in nature, and such parallel implementation of neural networks is hoped to be successfully extended for a large variety of *M* values.

This method adopts the famous technique of constructing a multiclass classification system using many single-class binary classifiers, with each classifier developed using all-against-one methodology. Hence, each BPNN authenticator is developed as a binary classifier where the class level is chosen as either +1 (for the signals pertaining to the correct water category under authentication) or −1 (corresponds to signals pertaining to all other water categories). Then, the binary classification problem for each authenticator module can be formulated on the basis of a given data set (Ω), with **x***i* input features and *di* classification output, of the form

$$\Omega = \{(\mathbf{x}1, d1), (\mathbf{x}2, d2). . . (\mathbf{XN}, Dn)\}$$

Where $\mathbf{x}i \in \_m$, $di \in \{+1,-1\}$, m is the dimension of the feature vector, and N is the number of training samples/exemplars.

A. BPNN-LM Algorithm

The BPNN-LM algorithm is popular for providing fast convergence in the training phase, provided that the system can support the memory requirements . They essentially employ multilayer perceptions with optimization techniques to train the free adaptable weights. In this algorithm, the cost function is formulated as the sum of squared errors over all exemplars (N) in the training data set, in a given epoch (k).

The LM algorithm for computing weight updates is given as

$$\mathbf{W}k+1 = \mathbf{w}k - [\mathbf{H}+ \mu\mathbf{I}]-1\mathbf{g}$$

Where $\mathbf{w}k$ = weight vector in kth epoch, $\mathbf{H}$ = the Hessian matrix, μ = the learning rate, and $\mathbf{g}$ = the gradient vector. Here, the Hessian matrix $\mathbf{H}$ can be approximated as and the gradient vector $\mathbf{g}$ can be computed as

$$\mathbf{H} = \mathbf{J}\mathrm{T}\mathbf{J}$$

$$\mathbf{g} = \mathbf{J}\mathrm{T}\mathbf{e}$$

Where $\mathbf{J}$ = the Jacobean matrix containing the first-order derivatives of the neural network errors with respect to weights and biases and $\mathbf{e}$ = the vector of neural network errors. This ensures that no explicit calculation of the Hessian matrix is required.

B. BPNN-RP Algorithm

The BPNN-RP algorithm is also popular for providing fast convergence. Let E be the sum of squared errors over all exemplars (N) in the training data set, in a given epoch (t), and let wij be the weight between the ith input node and jth output node between two successive layers. This variation of BPNN algorithm achieves convergence by adapting weights and biases, considering the polarities of $\partial E/\partial wij$ only and not considering the magnitude of $\partial E/\partial wij$. Here, each incremental weight Δwij (t) after tth epoch is determined by a fixed step Δij (t) whose sign, positive or negative, will be determined by the sign of $\partial E/\partial wij$. Hence, after each epoch t, all the weights and biases in

all layers get similarly affected. This is believed to be the driving force for this algorithm behind potential faster acceleration toward convergence.

4 CONCLUSION

This paper has proposed the development of a pulse- voltametry-method-based E-Tongue instrumentation system that can be successfully employed in real life for water sample authentication. The proposed system uses a hybrid combination of ST-based feature extractor, with BPNN-based binary classifiers, to develop an automated authentication tool. The system is developed as a parallel combination of several neural network classifiers, each dedicated to authenticate a specific category of water sample. The system can be logically extended for large categories of water samples. The system has been implemented in a laboratory environment for various water samples, commonly and commercially available in India, and the experimentations were performed for two types of working electrodes, silver and platinum. The authentication performances were largely found satisfactory, mostly in the upper 80% and often quite exceeding 90%. It was also found that merely increasing the number of features for development of the authentication system does not always really help, and in fact, in our system, it degraded the overall performance when the number of features was increased from 10 to 20.

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Area and Delay Efficient Digital Comparator

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Abstract

Quantum-dot cellular automata (QCA) tend to be an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. Efficient solutions have recently been proposed for several arithmetic circuits, such as adders, multipliers, and comparators. This paper proposes a new design approach oriented to the implementation of binary comparators in QCA. The proposed work uses novel implementation strategies, methodologies and new formulations of basic logic equations to make the comparison function applied to comparator efficient. The new strategy has been exploited in the design of two different comparator architectures and for several operands word lengths. The comparators proposed here exhibit significantly higher speed and reduced overall area. The existing and proposed comparators are synthesized using Xilinx and performance is evaluated in terms of number of gates and delay.

Key words: Binary comparators, majority gates, Quantum-dot cellular automata (QCA).

I. INTRODUCTION

Quantum-dot cellular automata (QCA) technology provides a promising opportunity to overcome the approaching limits of conventional CMOS technology [1]– [6]. For this reason, in recent years the design of logic circuits based on QCA received a great deal of attention, and special efforts have been directed towards arithmetic circuits, such as adders

[7]–[14],multipliers [15]–[21] and comparators [22]–[28].Even though comparators are key elements for a wide range of applications [29][30].QCA implementations existing in the literature are mainly provided for comparing two single bits. Only few examples of comparators able to process *n*-bit operands, with $n > 2$, are available [24][26][27].The comparator described in [22] simply computes the XNOR function to check whether two input bits *a* and *b* match each other. The structures proposed in [23]–[28] have higher computational capabilities, and circuits able to recognize all the three possible conditions in which $a = b$, $a > b$ and $a < b$ (full comparators) are described in [23][24]and [27]. The 1-bit implementation is proposed in [23] and then improved in [25], has been exploited in [27] to design a parallel *n*-bit full comparator. An example of serial structures is provided in [24], whereas the *n*-bit comparator described in [26] can recognize only the case in which, *A* and *B* being the *n* bit inputs, $A \geq B$.

With respect to other QCA designs, the latter exhibit reduced delays, area occupancy and number of used cells.

This paper focuses on the design of efficient parallel QCA based *n*-bit full comparators. The novel theorems were applied to achieve innovative QCA based structures of *n*-bit full comparators that were laid out and are synthesized using Xilinx Tool.

The rest of the paper is organized as follows: a brief background of the QCA design approach and existing QCA implementations of binary comparators is given in Section II; the proposed comparator based on new theorems and corollaries are then enunciated and demonstrated in Section III; Simulation results and comparison of performance is done in Section IV; Finally, in Section V, conclusion is presented.

II. BACKGROUND AND RELATED WORKS

The basic element of a nanostructure based on QCA is a square cell with four quantum dots and two free electrons. The latter can tunnel through the dots within the cell but owing to Coulombic repulsion, they will always reside in opposite corners [1], thus leading to only two

possible stable states, also named polarizations. Locations of the electrons in the cell are associated with the binary states 1 and 0. Adjacent cells interact through electrostatic forces and tend to align their polarizations. However, QCA cells do not have intrinsic data flow directionality. Therefore, to achieve controllable data directions, the cells within a QCA design are partitioned into the so-called clock zones that are progressively associated with four clock signals, each phase shifted by 90º. This clock scheme, named the zone clocking scheme, makes the QCA designs intrinsically pipelined, since each clock zone behaves like a D-latch [20].QCA cells are used for both logic structures and interconnections that can exploit either the coplanar cross or the bridge technique [1][2][6][31][32]. The fundamental logic gates inherently available within the QCA technology are the inverter and the majority gate (MG). Given three inputs *a, b* and *c*, the MG performs the logic function reported in [1] provided that all input cells are associated with the same clock signal *clkx* (with *x* ranging from 0 to 3), whereas the remaining cells of the MG are associated with the clock signal *clkx*+1

$$M(a, b, c) = a \cdot b + a \cdot c + b \cdot c \qquad (1)$$

There are several QCA designs of comparators in the literature [22]–[28]. A 1-bit binary comparator receives two bits *a* and *b* as inputs and establishes whether they are equal, less than or greater than each other. These possible states are represented through three output signals, here named *A*eq*B*,

*A*big*B*, *B*big*A*, that are asserted, respectively, when $a = b$, $a>b$, and $a<b$. Full comparators are those that can separately identify all the above cases, whereas non-full comparators recognize just one or two of them. As an example, the comparator designed in [22] and depicted in Fig. 1(a) can verify only whether $a = b$. Conversely, the circuits shown in **Fig. 1(b) and (c)**, proposed in [23] and [24] are full comparators. The latter also exploits two 1-bit registers *D* to process *n*-bit operands serially from the least significant bit to the most significant one. With the main objective of reducing the number of wire crossings, which is still a big challenge of QCA designs [33]–[35] in [25] the universal logic gate (ULG) $f(y1, y2, y3) = M(M(y1, y2 , 0), M(y1, y3 , 1), 1)$ was proposed and then used to implement the comparator illustrated in Fig. 1(d). It is worth noting that, two *n*-bit numbers $A(n-1:0) = an-1 \ldots a0$ and $B(n-1:0) = bn-1 \ldots b0$ can be processed by cascading *n* instances of the 1-bit comparator. Each instance receives as inputs the *i*th bits *ai* and *bi* (with $i = n - 1, \ldots, 0$) of the operands and the signals *A*big*B*($i-$ 1:0) and *B*big*A*($i-$ 1:0) . The former is asserted when the subword $A(i-1:0) = ai-1 \ldots a0$ represents a binary number greater than $B(i-1:0) = bi-1 \ldots b0$. In a similar way, *B*big*A*($i-1$:0) is set to 1 when $A(i-1:0) < B(i-1:0)$. The outputs *A*big*B*(*i*:0) and *B*big*A*(*i*:0) directly feed the next stage.

It can be seen that this circuit does not identify the case in which $A = B$, therefore it cannot be classified as a full- comparator.

With the main objective of reducing the number of wire crossings, which is still a big challenge of QCA designs [33]–[35], in [25] the universal logic gate (ULG) $f(y1, y2, y3) = M(M(y1, y2 , 0), M(y1, y3 , 1), 1)$ was proposed and then used to implement the comparator illustrated in Fig. 1(d). It is worth noting that, two *n*-bit numbers $A(n-1:0) = an-1 \ldots a0$ and $B(n-1:0) = bn-1 \ldots b0$ can be processed by cascading *n* instances of the 1-bit comparator. Each instance receives as inputs the *i*th bits *ai* and *bi* (with $i = n - 1, \ldots, 0$) of the operands and the signals *A*big*B*($i-1$:0) and *B*big*A*($i-1$:0) . The former is asserted when the subword $A(i-1:0) = ai-1 \ldots a0$ represents a binary number greater than $B(i-1:0) = bi-1 \ldots b0$. .In a similarway, *B*big*A*($i-1$:0) is set to 1 when $A(i-1:0) < B(i-1:0)$. The outputs *A*big*B*(*i*:0)

and *B*big*A*(*i*:0) directly feed the next stage. It can be seen that this circuit does not identify the case in which $A = B$, therefore it cannot be classified as a full-comparator.

The design described in [26] exploits a tree-based (TB) architecture and exhibits a delay that in theory logarithmically increases with n. The 2-bit version of such designed comparator is illustrated in Fig. 1(e).

Also the full comparator proposed in [27] exploits a TB architecture to achieve high speed. As shown in Fig. 1(f), where 4-bit operands are assumed, one instance of the 1-bit comparator presented in [23] is used for each bit position. The intermediate results obtained in this way are then further processed through a proper number of cascaded 2-input OR and AND gates implemented by means of MGs having one input permanently set to 1 and 0, respectively.

Analyzing existing QCA implementations of binary comparators it can be observed that they were designed directly mapping the basic Boolean functions consolidated for the CMOS logic designs to MGs and inverters, or ULGs. Unfortunately, in this way the computational capability offered by each MG could be underutilized [13][36][37]. As a consequence, both the complexity and the overall delay of the resulting QCA designs could be increased in vain.

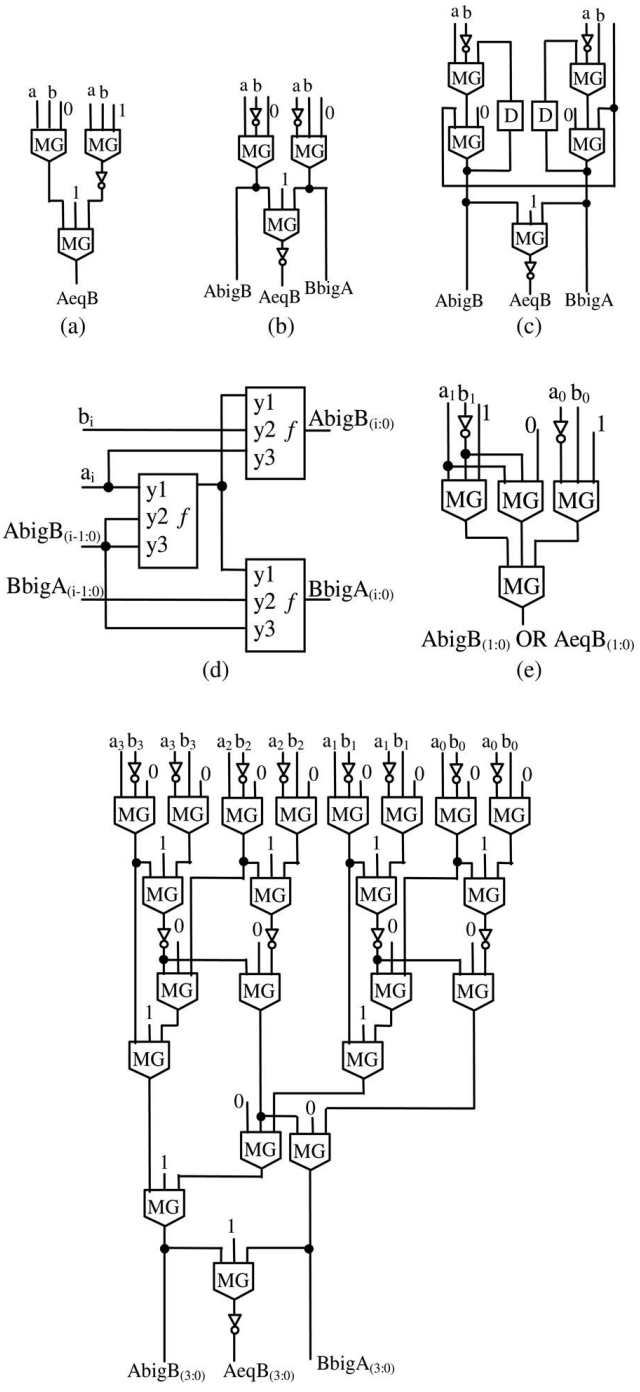


Fig. 1. QCA-based comparators presented in: (a) [22]; (b) [23]; (c) [24];(d) [25]; (e) [26]; (f) [27].

III. THEOREMS AND COROLLORIES OF *n*-BIT FULL COMPARATORS

In this section, four original theorems and two corollaries are enunciated that can significantly increase the speed performances of QCA-based designs of full comparators and can significantly reduce the number of used MGs and inverters with respect to existing comparators, thus reducing also the number of used cells and the overall active area.

The novel formulations can be exploited in the design of *n*-bit full comparators splitting the operands $A(n-1:0) = a_{n-1} \ldots a_0$ and $B(n-1:0) = b_{n-1} \ldots b_0$ into a proper number of 2-bit and 3-bit subwords that can be compared applying Theorems 1 and 2. The intermediate results obtained in this way can be then further processed by applying Theorems 3 and 4 together with Corollaries 1 and 2.

Theorem 1:

If $A(k-1:k-2) = a_{k-1}a_{k-2}$ and $B(k-1:k-2) = b_{k-1}b_{k-2}$,with $k = 2, 4, \ldots, n-2, n$, are two 2-bit subwords of the *n*-bit numbers $A(n-1:0)$ and $B(n-1:0)$, respectively, then $A\text{big}B(k-1:k-2)$ as defined in (2) is equal to 1 if and only if $A(k-1:k-2) > B(k-1:k-2)$; $B\text{big}A(k-1:k-2)$ as defined in (3) is equal to 0 if and only if $A(k-1:k-2) < B(k-1:k-2)$.

$$A_{\text{big}}B_{(k-1:k-2)} = M\left(a_{k-1}, \overline{b_{k-1}}, a_{k-2}\right) \cdot M\left(a_{k-1}, \overline{b_{k-1}}, \overline{b_{k-2}}\right) \quad (2)$$

$$\overline{B_{\text{big}}A_{(k-1:k-2)}} = M\left(a_{k-1}, \overline{b_{k-1}}, a_{k-2}\right) + M\left(a_{k-1}, \overline{b_{k-1}}, \overline{b_{k-2}}\right) \quad (3)$$

Theorem 2:

If $A(k-1:k-3) = a_{k-1}a_{k-2}a_{k-3}$ and $B(k-1:k-3) = b_{k-1}b_{k-2}b_{k-3}$, with $k = 3, 6, \ldots, n-3, n$, are 3-bit subwords of the *n*-bit numbers $A(n-1:0)$ and $B(n-1:0)$, respectively, then $A\text{big}B(k-1:k-3)$ as defined in (4) is equal to 1 if and only if $A(k-1:k-3) > B(k-1:k-3)$; $B\text{big}A(k-1:k-3)$ as given in (5) is equal to 0 if and only if $A(k-1:k-3) < B(k-1:k-3)$.

$$A_{\text{big}}B_{(k-1:k-3)} = M(M\left(a_{k-1}, \overline{b_{k-1}}, a_{k-2}\right), M\left(a_{k-1}, \overline{b_{k-1}}, \overline{b_{k-2}}\right), a_{k-3} \cdot \overline{b_{k-3}}) \quad (4)$$

$$\overline{B_{\text{big}}A_{k-1:k-3}} = M(M\left(a_{k-1}, \overline{b_{k-1}}, a_{k-2}\right), M\left(a_{k-1}, \overline{b_{k-1}}, \overline{b_{k-2}}\right), a_{k-3} + \overline{b_{k-3}}). \quad (5)$$

Theorem 3:

Given two *n*-bit numbers *A*(*n*−1:0) and *B*(*n*−1:0) ,(6) gives *A*big*B*(*n*−1:0) = 1 if and only if *A*(*n*−1:0) > *B*(*n*−1:0) , whereas (7) gives *B*big*A*(*n*−1:0) = 0 if and only if *A*(*n*−1:0) < *B*(*n*−1:0).

$$A_{\text{big}}B_{(n-1:0)} = M(M\left(a_{n-1}, \overline{b_{n-1}}, a_{n-2}\right), M\left(a_{n-1}, \overline{b_{n-1}}, \overline{b_{n-2}}\right), A_{\text{big}}B_{(n-3:0)}) \quad (6)$$

$$\overline{B_{\text{big}}A_{(n-1:0)}} = M(M\left(a_{n-1}, \overline{b_{n-1}}, a_{n-2}\right), M\left(a_{n-1}, \overline{b_{n-1}}, \overline{b_{n-2}}\right), \overline{B_{\text{big}}A_{(n-3:0)}}) \quad (7)$$

Theorem 4:

If *A*(*n*−1:0) and *B*(*n*−1:0) are two *n*-bit numbers,then

*A*big*B*(*n*−1:*n*−3) and *B*big*A*(*n*−1:*n*−3) being computed by (4) and

(5), respectively, then Abig$B(n-1{:}0)$ as defined in (8) is equal to 1 if and only if $A(n-1{:}0) > B(n-1{:}0)$, whereas Bbig$A(n-1{:}0)$ as defined in (9) is equal to 0 if and only if $A(n-1{:}0) < B(n-1{:}0)$.

$$A_{\text{big}}B_{\langle n-1:0\rangle} = M\left(A_{\text{big}}B_{\langle n-1:n-3\rangle}, \overline{B_{\text{big}}A_{\langle n-1:n-3\rangle}}, A_{\text{big}}B_{\langle n-4:0\rangle}\right) \quad (8)$$

$$\overline{B_{\text{big}}A_{\langle n-1:0\rangle}} = M\left(A_{\text{big}}B_{\langle n-1:n-3\rangle}, \overline{B_{\text{big}}A_{\langle n-1:n-3\rangle}}, \overline{B_{\text{big}}A_{\langle n-4:0\rangle}}\right). \quad (9)$$

Corollary 1:

Let's consider two n-bit numbers $A(n-1{:}0)$ and $B(n-1{:}0)$, and let's suppose that they are split into the subwords $A(n-1{:}h)$,$A(h-1{:}0)$,$B(n-1{:}h)$ and $B(h-1{:}0)$.If Abig$B(n-1{:}h)$, Abig$B(h-1{:}0)$, Bbig$A(n-1{:}h)$ and Bbig$A(h-1{:}0)$ are computed by applying Theorems 3 and 4, then Abig$B(n-1{:}0)$ as defined in (10) is equal to 1 if and only if $A(n-1{:}0) > B(n-1{:}0)$, whereas Bbig$A(n-1{:}0)$ as defined in (11) is equal to 0

$$A_{\text{big}}B_{\langle n-1:0\rangle} = M\left(A_{\text{big}}B_{\langle n-1:h\rangle}, \overline{B_{\text{big}}A_{\langle n-1:h\rangle}}, A_{\text{big}}B_{\langle h-1:0\rangle}\right) \quad (10)$$

$$\overline{B_{\text{big}}A_{\langle h-1:0\rangle}} = M\left(A_{\text{big}}B_{\langle n-1:h\rangle}, \overline{B_{\text{big}}A_{\langle n-1:h\rangle}}, \overline{B_{\text{big}}A_{\langle h-1:0\rangle}}\right) \quad (11)$$

if and only if $A(n-1{:}0) < B(n-1{:}0)$.

Corollary 2:

Given two n-bit numbers $A(n-1{:}0)$ and $B(n-1{:}0)$, if Abig$B(n-1{:}0)$ and Bbig$A(n-1{:}0)$ are computed by applying Theorems 1, 2, 3, and 4 and/or Corollary 1, then Aeq$B(n-1{:}0)$ defined in (12) is equal to 1 if and only if $A(n-1{:}0) = B(n-1{:}0)$.

$$A_{\text{eq}}B_{\langle n-1:0\rangle} = M\left(\overline{A_{\text{big}}B_{\langle n-1:0\rangle}}, \overline{B_{\text{big}}A_{\langle n-1:0\rangle}}, 0\right). \quad (12)$$

In order to exploit the novel approach, the operands $A(n-1{:}0)$ and $B(n-1{:}0)$ are split into a proper number of 2- and 3-bit subwords that are compared applying Theorems 1 and 2.The results obtained comparing 2- and 3-bit subwords are then combined by applying Theorems 3 and 4 together with Corollaries 1 and 2.

IV. PROPOSED BINARY COMPARATOR

The circuits illustrated in Fig. 2 were designed to implement in QCA the novel equations demonstrated in the previous Section. The generic module Ti, with *i* ranging between 1 and 4, implements the equations enunciated in the *i*th *theorem*,whereas C1 and C2 compute the signals *A*big*B*(*k*−1:0),*B*big*A*(*k*−1:0), and *A*eq*B*(*k*−1:0) as shown above in Corollaries 1 and 2, respectively. As examples of application, the above QCA modules have been used to design two different structures of full comparators named cascade-based and TB architectures. However, many other structures can be designed by combining the basic modules in different manners.

A) Novel QCA Comparators

The first proposed comparator exploits a cascade-based (CB) architecture. To explain better how the overall

computation is performed, the schematic diagram illustrated in Fig. 3 is provided. It shows a possible implementation of a

32-bit comparator based on the proposed theory.

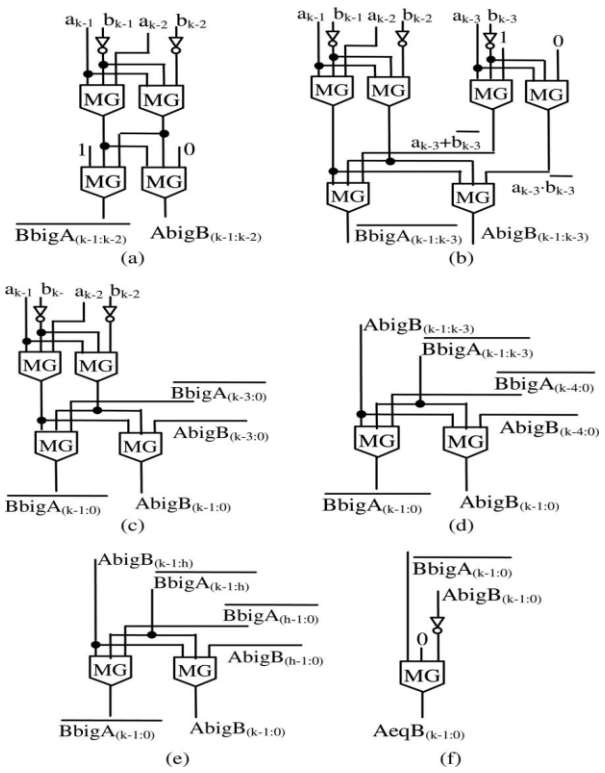


Fig. 2. QCA modules: (a) T1; (b) T2; (c) T3; (d) T4; (e) C1; and (f) C2.

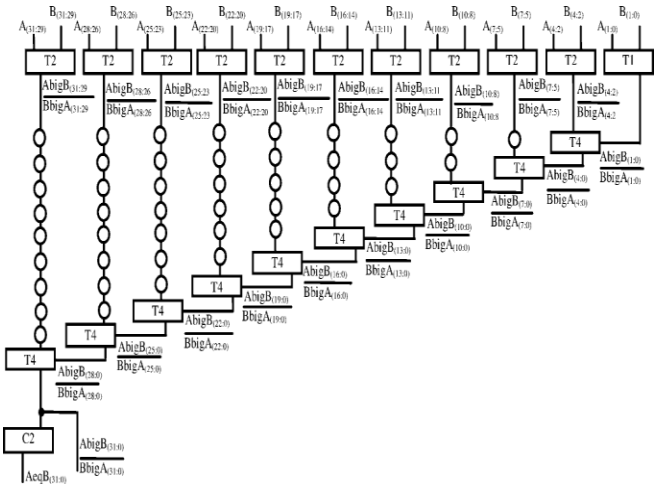


Fig. 3. Novel 32-bit CB full comparator.

Circles visible in Fig. 3 indicate the additional clock phases that have to be inserted on wires to guarantee the correct synchronization of the overall design. The CB full comparator was designed for operands word lengths ranging from 2 to 32 and using, for $n > 2$, the split criterion summarized in Table I. Obviously, alternative splits could be used.

TABLE I

SPLITTING CRITERION ADOPTED IN THE CB COMPARATORS

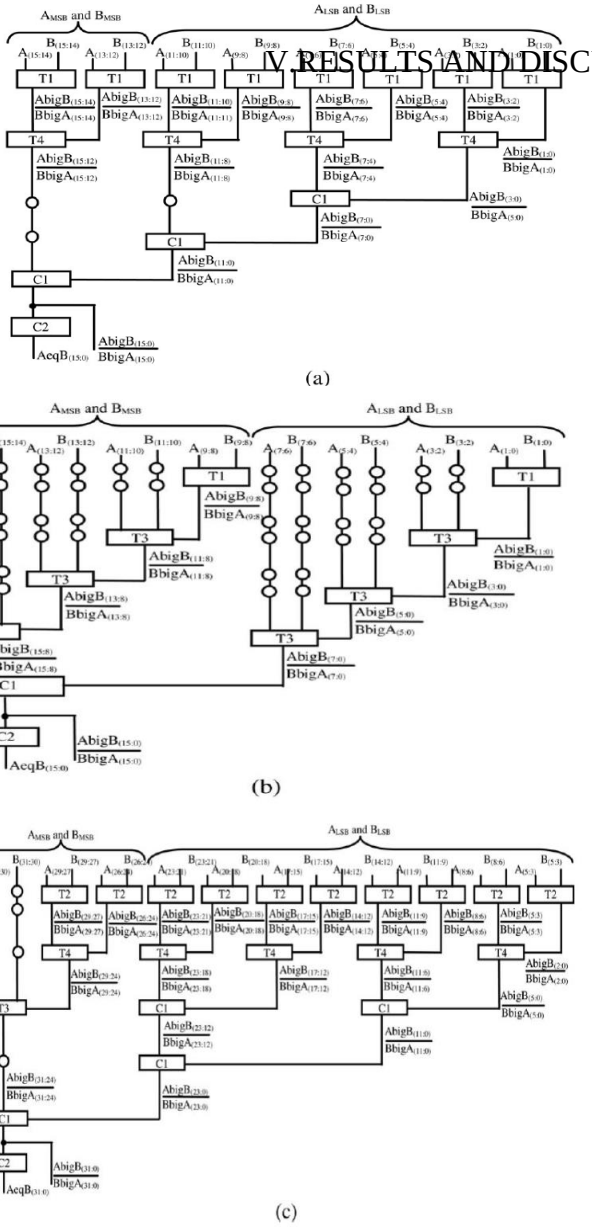
n	*Splitting of the operands*
4	$A_{(3:2)}A_{(1:0)}$ $B_{(3:2)}B_{(1:0)}$
8	$A_{(7:5)}A_{(4:2)}A_{(1:0)}$ $B_{(7:5)}B_{(4:2)}B_{(1:0)}$
16	$A_{(15:14)}A_{(13:11)}A_{(10:8)}A_{(7:5)}A_{(4:2)}A_{(1:0)}$
	$B_{(15:14)}B_{(13:11)}B_{(10:8)}B_{(7:5)}B_{(4:2)}B_{(1:0)}$
32	$A_{(31:29)}A_{(28:26)}A_{(25:23)}A_{(22:20)}A_{(19:17)}A_{(16:14)}A_{(13:11)}A_{(10:8)}A_{(7:5)}A_{(4:2)}A_{(1:0)}$
	$B_{(31:29)}B_{(28:26)}B_{(25:23)}B_{(22:20)}B_{(19:17)}B_{(16:14)}B_{(13:11)}B_{(10:8)}B_{(7:5)}B_{(4:2)}B_{(1:0)}$

As it is well known, the number of cascaded MGs within the worst computational path of a QCA design directly affects the delay achieved. In fact, each MG introduces one clock phase in the overall delay. From Fig. 2, it can be seen that the modules T1 and T2 contribute to the computational path with one inverter and two MGs. Each instance of T4 introduces one more MG, whereas C2 is responsible for one MG and one inverter. As a consequence, the critical computational path of the novel *n*-bit CB full comparator consists of *n*/3+ 3 MGs and 2 inverters. As an example, the 32-bit implementation depicted in Fig. 3 has the worst-case path made up of 13 MGs and 2 inverters. The number of MGs within the computational path of the above described comparator linearly increases with *n*. An alternative solution presented here adopts a TB architecture to achieve shorter computational paths. When this approach is exploited, several implementations of an *n*-bit full comparator can be designed differently combining the novel theorems and corollaries, as well as their QCA implementations depicted in Fig. 2.

The TB comparators implement the comparison function recursively. The operands *A* and *B* are preliminarily partitioned as *A* = *A*MSB*A*LSB and *B* = *B*MSB*B*LSB. The portions *A*MSB and *B*MSB are compared independently of the portions *A*LSB and *B*LSB. The depth of the recursion directly impacts the whole architecture. Examples of TB structures designed for 16- and 32-bit comparators are illustrated in Fig. 4. In Fig. 4(b) and (d), the recursion with its minimum depth is adopted. The portions *A*MSB and *B*MSB, as well as the portions *A*LSB and *B*LSB, are separately compared trough two independent CB architectures. The overall result is

finally built with the modules C1 and C2. Fig. 4(a) and (c) shows comparators designed adopting deeper recursions. In the following of the paper, the 16- and 32-bit TB implementations illustrated in Fig. 4(b) and (d) are deeply analyzed. Referring to the QCA modules depicted in Fig. 2, it can be easily verified that the former uses 35 MGs and 17 inverters and its critical computational path consists of 7 MGs and 2 inverters, whereas the latter utilizes 83 MGs and 33 inverters and it has a worst-case path composed by 9 MGs and 2 inverters.

V. RESULTS AND DISCUSSION



The performance of the tree based and cascade based architectures are compared in terms of number of gates.The cascade based approach uses large number of MGs compared to Tree based approach.

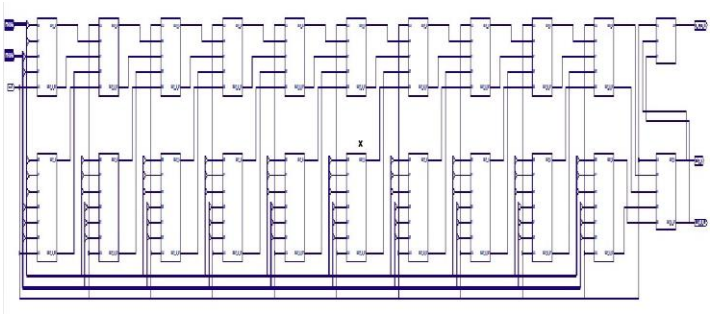


Fig. 5. Equivalent Cascade based comparator RTL diagram

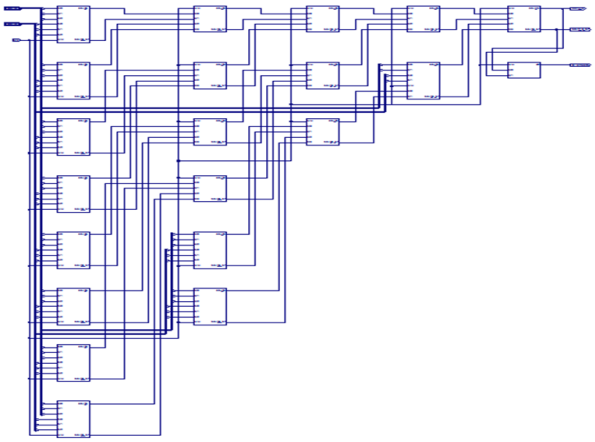
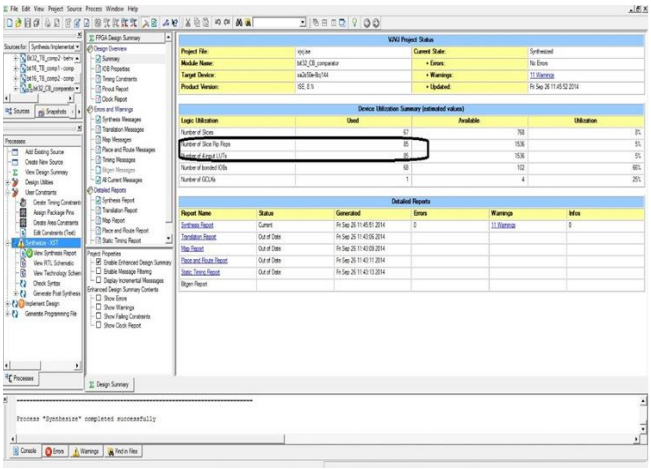


Fig. 6. Equivalent Tree based comparator RTL diagram



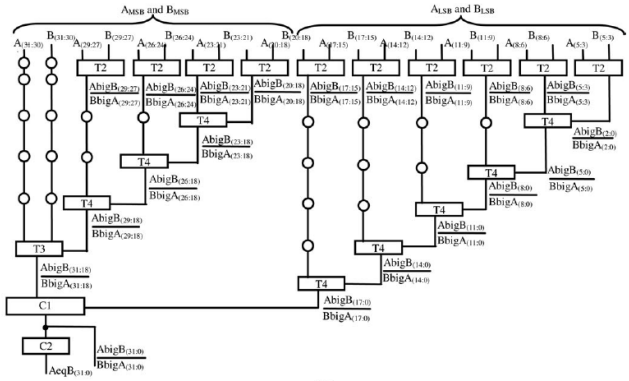


Fig. 4. Examples of novel TB comparators with: (a) and (b) 16- bit operands; (c) and (d) 32-bit inputs.

Fig. 7. Synthesis result for Cascade based comparator

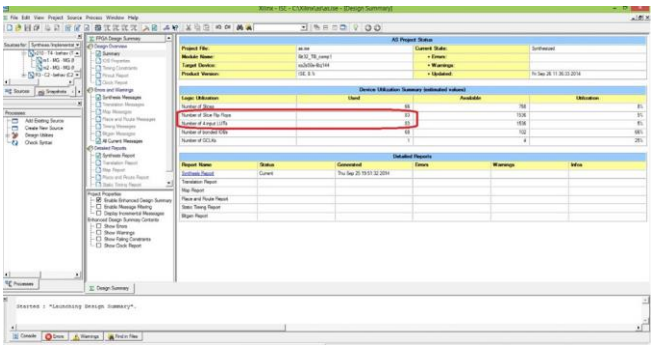


Fig. 7. Synthesis result for Tree based comparator

TABLE II RESULTS

IV. CONCLUSION

A new methodology useful to design binary comparators in QCA has been presented. The novel comparators split the received *n*-bit inputs into a proper number of 2- and 3-bit subwords that are processed in parallel through 2- and 3-bit comparators designed by applying theorems demonstrated here. The proposed TB architecture is efficient compared to CB architecture.

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Stability Analysis of Laminated Composite Plates with an Elliptical/Circular/Square Cut-out using FEM

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Abstract

This paper addresses the effects of a cut-out on the buckling behaviour of square plates made of polymer matrix composites (PMC). The study is concentrated on the behaviour of square symmetric cross-ply laminates. The laminated plates were symmetrically orderly arranged into the following way [0/90]2S.The resistance to buckling of the laminated plates subjected to mono-axial compression is highlighted according to effect of boundary condition; the unloaded edges are modelled in clamped and simply supported boundary condition. Finite element analysis is performed to predict the effects of cut out of circular, square and elliptical hole aligned in along the loading direction and aligned in perpendicular to the loading direction on the buckling behaviour of these plates.

Key words: stability analysis, laminated composite plates, FEM cut out.

1. Introduction

Application fields of composite materials are continuously expanding, from traditional application areas such as military aircraft to various engineering fields including commercial aircrafts, automobiles, robotic arms and even architecture [1]. The correct understanding of their structural behaviour is necessary, such as the deflections, buckling loads and modal characteristics, the through-thickness distributions of stresses and strains, the large deflection behaviour and, of extreme significance for obtaining strong, reliable multi-layered structures, the failure characteristics [2]. Throughout operation the composite laminate plates are generally subjected to compression loads that may basis buckling if overloaded. Consequently their buckling behaviours are significant factors in safe and reliable design of these structures [3]. For predicting the buckling load and buckling mode form of a structure in the finite element program, the linear (or eigenvalue) buckling analysis is an existing technique for estimation [4]. In general, the analysis of composite laminated plates is more complicated than the analysis of homogeneous isotropic ones [5]. In the literature, there are a range of published studies on the buckling of composite plates. Akbulut and Sayman [6] carried out a buckling analysis of a rectangular composite laminates with a central square hole. Using the first order shear deformation theory, the critical buckling loads of composite plates which were designed as symmetric angle-ply, antisymmetric cross-ply or angle ply under the in plane loads were found for constant or various thicknesses, simple or clamped boundary conditions, various modules ratios, simple or biaxial loading versus hole sizes. Kundu and Sinha [7] performed the geometrically nonlinear post buckling analysis of laminated composite doubly curved shells by finite element method.

The principle of virtual work forms the origin to derive the nonlinear finite element equations. Kong et al. [8] analysed buckling and post buckling behaviours both numerically and experimentally for composite plates with a hole. In the finite element analysis, the updated Lagrangian formulation and the eight-node degenerated shell element were used. The effect of hole sizes and stacking sequences was examined on the compression behaviour of the plate. Experiments showed fine agreement with the finite element results in the buckling load and the post buckling strength. Ghannadpour et al. [9] studied the influences of a cut out on the buckling performance of rectangular plates made of polymer matrix composites (PMC). The study was concentrated on the behaviour of rectangular symmetric cross-ply laminates. Finite element analysis was also carried out to obtain the effects of cut out on the buckling behaviour of these plates. Jain and Kumar [10] carried out the finite element method for the post buckling response of symmetric square laminates with a central cut out under uniaxial compression. The governing finite element equations were solved using the Newton–Raphson method. For the purpose of analysis, laminates with circular and elliptical cut outs were considered with a view to investigate the effect of cut out shape, size and the alignment of the elliptical cut out on the buckling and the first-ply failure loads of laminates. The buckling response of a woven/glass/polyester composite laminated square plate with elliptical hole is investigated by Komur et al. [11] using ANSYS code. They indicated that the designer must avoided the big elliptical holes in laminated composite plates, if it is wanted to prevent buckling loads at lower pressures. Hamani et al. [12] have determined the effect of fibre orientation on the critical buckling load of symmetrical laminated composite plates having a crack emanating from a circular notch. They pointed out that the critical buckling loads attain important maximum values when the fibres are oriented in the range of 50^{o}_90^{o} whereas the minimum values are obtained when the fibres are perpendicular to the applied pressure. In this paper the effect of circular and elliptical cut outs on the buckling behaviour of composite plates in cross-ply laminates are taken in to consideration. This study also contains the effect of circular cut out size in different plate aspect ratios on the buckling behaviour of the cross-ply laminated composite plates.

2. Finite Element Modelling

In this study, the square plate cross-ply laminate [0, 90]2s is considered. The length and width of the composite plate is 120mmX120mm. The plate is constituted of eight plies, each having a thickness of 0.125mm.The properties of the material of the lamina are E1=130GPa, E2=10Gpa, E3=10GPa, G12=G13=5Gpa, G23=3.375Gpa. v12 = v13 = 0.35, v23 = v32=0.49.The finite element commercial code ANSYS APDL 11.0 has been used for the analysis. The plate normal is aligned in z direction and plate area is located on XY plane. The simply supported boundary conditions are applied on each four edges by fixing the translational displacement in z axis. The compression load is applied uniformly along the two opposite edges. These plates are meshed with quadratic and triangular Elements by programme chosen option as illustrated in Fig.1. In order to achieve the static equilibrium, four nodes at the middle point of each edge are fixed i.e. the displacements in y direction are fixed in loaded edges along with the displacements in x direction are fixed in transverse sides.

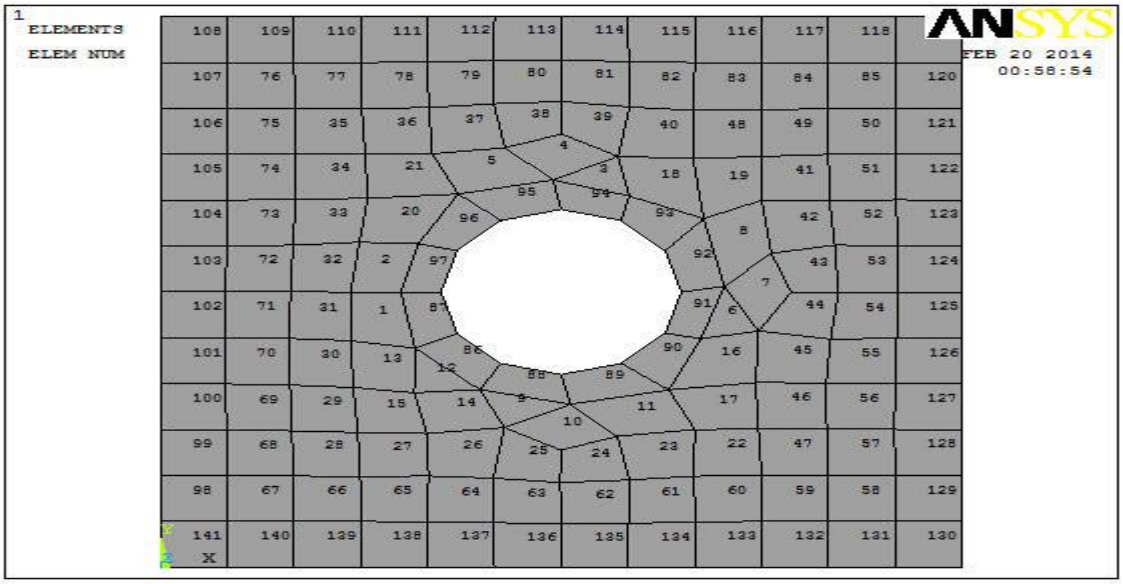

Fig.1. Typical mesh for a cross-ply square laminated plate with circular cut out

3. Effect of Cut Out Size

In this section the effect of circular cut out size and square cut out size is taken in to consideration. The plate dimension is 120 x120 mm. Table 1 gives the non-dimensional buckling loads for cross-ply laminated composite plates with the cut out diameter to the laminate width ratio (d/b) and square width (c) to laminate width (b) ratio are given in Table 2. The results of Table 1 are displayed in Fig. 2.the buckling load for the square plate with circular cut out is having higher buckling load than in square cut out in same ratios.

Table 1

Cross-ply laminate with a circular and square cut out

Buckling load (N)			
d/b	b_1/b	Circular	Square
0.1	0.1	15.457	14.622
0.3	0.3	9.7650	9.4550
0.5	0.5	8.0036	6.7082
0.8	0.8	6.8647	5.3715
0.9	0.9	4.892	4.4513

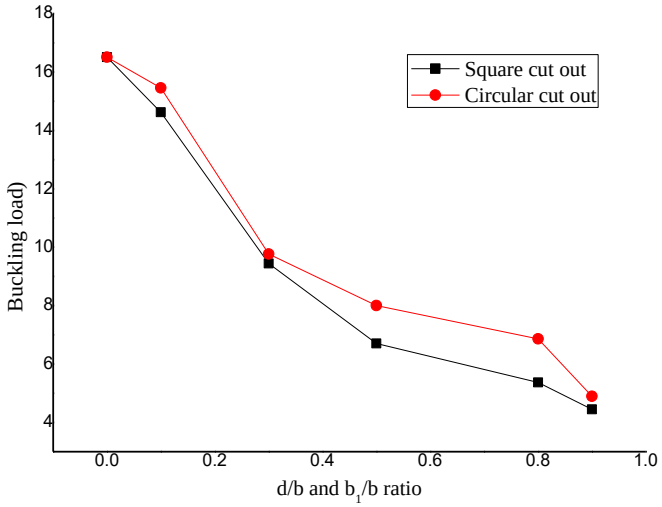

Fig.2. Variation of buckling loads with square and circular cut outs

4. Effect of Cut Out Shape

In real applications of composite plates, different forms of the notch can be used for design purposes. The form of the notch was assumed to be an elliptical hole centered in the plate. In this section the effect of elliptical cut out is taken in to account. It is assumed that cut out to be located at the centre line of the square plates. The Direction of the loads and its boundary conditions are the same as previous section. The diameter of the ellipse which is aligned in load direction represented by e and the other diameter in transverse direction is represented by c. This investigation covers two types of elliptical cut outs. The first one investigating the elliptical cut outs which major diameter is aligned in load direction (x axis) and second one is for studying the ellipse which the minor diameter is aligned to the load direction (y axis).For the former type the value of e/b = 0.5 is constant and the value of c/b change from 0.0 to 0.5. For the later type the value of c/b = 0.5 is fixed and e/b varies from 0.0 to 0.5. Table 2 represents the variation of non-dimensional buckling loads in fixed c/b and different e/b. It is seen that the larger area of cut out causes the lower buckling load. The results of constant e/b and variable c/b are represented in Table 3. It is seen that the buckling load also decrease with increase of cut out area. Fig. 3 depicts the variation of elliptical cut out in axial and transverse loading direction. Results show that in the same cut out area, one which extended in perpendicular load direction has a higher buckling load compare to the cut outs that are located in transverse direction.

Table 2

Cross-ply laminate with an elliptical cut out (aligned along loading direction)

c/b	e/b	Buckling load (N)
0	0	16.508
0.5	0.05	10.453
0.5	0.15	9.6640
0.5	0.25	8.5070

0.5	0.35	8.1975
0.5	0.45	8.1067
0.5	0.5	8.0036

Table 3

Cross-ply laminate with an elliptical cut out (aligned in the perpendicular direction of loading)

e/b	c/b	Buckling load (N)
0	0	16.508
0.5	0.05	16.372
0.5	0.15	14.595
0.5	0.25	13.016
0.5	0.35	10.755
0.5	0.45	8.7160
0.5	0.5	8.0036

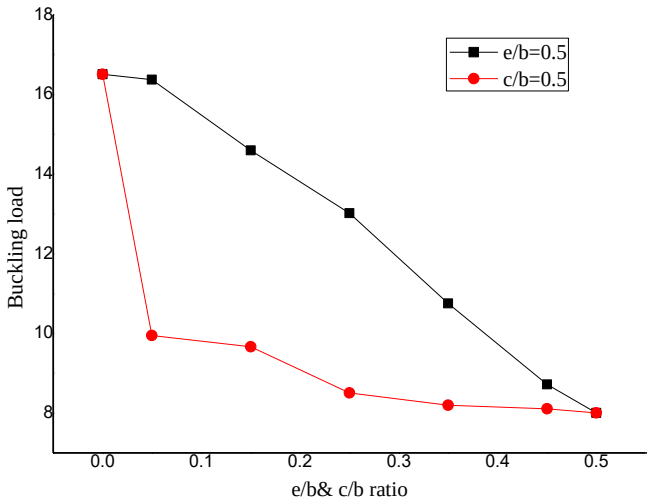

Fig.3.Variation of buckling loads with elliptical cut outs

5. Effect of Plate Aspect Ratio

This section deals with the buckling behaviour of perforated cross-ply laminated plates in different plate aspect Ratios. In this study the plate aspect ratios is selected to have integer value i.e. a/b = 1, 2, 3. Simply supported Boundary conditions are applied on four edges. The widths of these plates are equal to 120 mm, and all of the cut outs are positioned in the centre of the plates. The results of bulking loads in different cut out size are depicted in Fig.4.As mentioned before, the buckling loads of the square plate decreases with the cut out dimensions. Results show that the buckling load for the aspect ratio of 2 increases with increasing the cut out size but aspect ratio of 3, it is reduced up to d/b = 0.4 and increased for the d/b > 0.4 One can mention that applying the cut out on the rectangular plates can be improved by plate aspect ratio.

Table 4

Cross-ply laminate with various aspect ratios

S.No	d/b ratio	Buckling load (N)		
		a/b=1	a/b=2	a/b=3
1	0	16.508	16.529	16.534
2	0.2	12.199	17.652	15.080
3	0.3	9.7650	17.686	14.730
4	0.4	9.6776	17.915	14.426
5	0.6	8.1443	18.672	16.778
6	0.8	6.8647	19.960	20.340
7	0.9	4.892	25.368	22.674

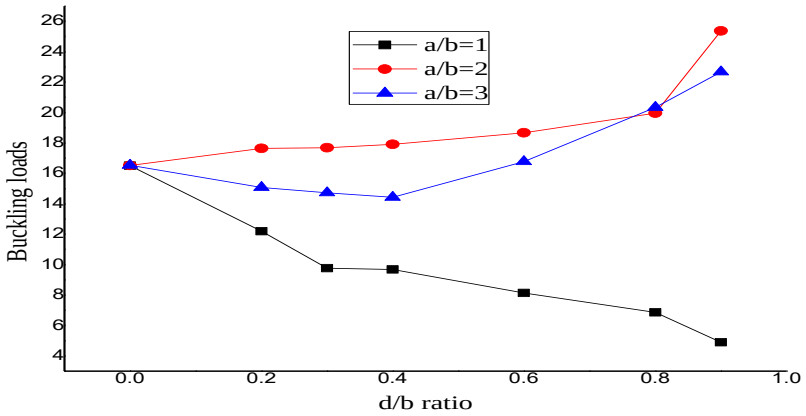

Fig.4.Variation of buckling loads with circular cut out dimensions in different plate aspect ratios

6. Effect of Boundary Condition

The boundary condition has a significant effect on buckling loads. In this study the cross-ply laminated plates is evaluated at two different boundary conditions, first case is simply supported in four edges; second case is simply supported in loaded edges and clamped in unloaded edges. The size of the perforated square plates is 120 mm. Fig. 5 displays the results of buckling load in different cut out size. Because of the rigidity of clamped boundary condition the buckling load is higher than simply supported boundary condition.

Table 4

Cross-ply laminate with various boundary conditions

S.No	d/b ratio	Buckling load (N)

		Simply supported	Clamped
1	0	16.508	16.529
2	0.2	12.199	17.652
3	0.3	9.7650	17.686
4	0.4	9.6776	17.915
5	0.6	8.1443	18.672
6	0.8	6.8647	19.960
7	0.9	4.892	25.368

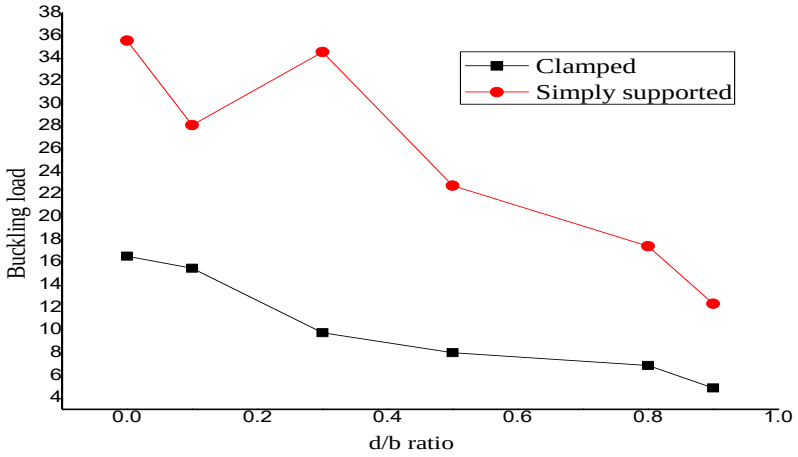

Fig.5.Variation of buckling loads in plate with different boundary conditions

7. Conclusion

Based on the results of the present investigations on buckling behaviour of square perforated composite Plates under compression load, the following conclusion can be made:

- The buckling load of the square plates containing a circular cut out reduces by the increment of cut out diameter.
- The buckling load for the square plate with circular cut out is having higher than the square plate with square cut out.
- Small cut outs can be neglected from modelling and can reduce the meshing efforts.
- In the elliptical cut outs, one which aligned perpendicular to load direction represents higher buckling load than one aligned in the direction of load.
- By selecting the integer value for plate aspect ratio the buckling load is increased by selecting the higher value for aspect ratio.
- The buckling load of perforated plates is highly influenced by its boundary conditions. The buckling load for the plate with clamped boundary condition on unloaded edges is 2 times higher than the buckling load for the plate with simply supported boundary condition.

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A Secure Routing Protocol for Mobile Ad hoc Network

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Abstract

To secure a mobile ad hoc network (MANET) inadversarial environment, a particularly challenging problem is how to feasibly detect and defend possible attacks on routing protocols, particularly internal attacks, such as a Byzantine attack. In this paper, we propose a novel algorithm that detects internal attacks by using both message and route redundancy during route discovery. The route-discovery messages are protected by pair wise secret keys between a source and destination and some intermediate nodes along a route established by using public key cryptographic mechanisms. We also propose an optimal routing algorithm with routing metric combining both requirements on a node's trustworthiness and performance. A node builds up the trustworthiness on its neighboring nodes based on its observations on the behaviors of the neighbor nodes. Both of the proposed algorithms can be integrated into existing routing protocols for MANETs, such as ad hoc on demand distance vector routing (AODV) and dynamic source routing (DSR). As an example, we present such an integrated protocol called secure routing against collusion (SRAC), in which a node makes a routing decision based on its trust of its neighboring nodes and the performance provided by them. The simulation results have demonstrated the significant advantages of the proposed attack detection and routing algorithm over some known protocols**.**

Key words: Secure Routing Protocol, Mobile Ad hoc Network.

1. INTRODUCTION

Mobile Ad hoc Networks

As the popularity of mobile devices and wireless networks significantly increased over the past years, wireless ad hoc networks has now become one of the most vibrant and active fields of communication and networking research. Given many intriguing future applications, there are still some critical challenges and open problems to be solved.

QOS is a guarantee by the network to provide certain performance for a flow in terms of the quantities of bandwidth, delay, jitter, packet loss probability etc. Ad hoc networks make the appear an even more challenging problem than ever before, despite some of re-active routing protocols can be configured to return only paths that comply with certain desired parameters. Bandwidth is seriously limited. Our ultimate goal is to provide a model from the application layer to the MAC layer for supporting service differentiation. A transport layer protocol to support different data streams, queue management and a -supported MAC will be addressed in our future work.

The main challenges in assuring MANET networks are due to the fact that a mobile link is susceptible to attacks, and node mobility renders the networks to having a highly dynamic topology. The attacks against routing protocols can be categorized into external and internal attacks. An external attack originates from a router that does not participate in the routing process but masquerades as a trusted router. They can either advertise false routing information or generate floods of spurious service requests, such as a denial of service (DOS) attack. An internal attack originates from a compromised, misconfigured, faulty, or even malicious router inside a network domain. Among the internal attacks, *Byzantine attacks* can be defined as attacks against routing protocols, in which two or more routers collude to drop, fabricate, modify, or misroute packets in an attempt to disrupt the routing services.

II. RELATED WORKS

The current secure routing protocols for MANETs can roughly be divided into two categories, i.e., 1) those adding security mechanisms to the existing routing protocols and 2) those designed to detect and defend specific attacks. In the first category, the common practice is to secure the popular on-demand routing protocols, such as ad hoc on-demand distance vector routing (AODV), destination sequenced distance vector (DSDV), and dynamic source routing

(DSR), by using a security association between the source and destination nodes such as pairwise secret keys and end-to-end authentication.

III. DYNAMIC KEY MANAGEMENT SCHEME AND ATTACK DETECTION ALGORITHM

We assume that a network is equipped with several security mechanisms in different layers in addition to the network layer. For example, the application layer can have some effective intrusion detection systems to monitor anomaly behaviors that can be used to detect and defend attacks such as DOS. In the network layer, the most possible attacks are data and routing information tampering. The majority of external attacks against routing protocols can be prevented by simple link layer encryption and authentication. We propose to have every node share a unique symmetric key with the source if it needs to transmit data. By applying this mechanism, the Sybil attack, the majority of selective forwarding and sinkhole attacks, and the HELLO flood attacks can be prevented. The major classes of attacks not countered are internal attacks and wormhole attacks. The defense mechanism for wormhole attacks can be found in. Therefore, we focus on internal attacks that are caused by authenticated routers, such as Byzantine attacks.

Dynamic Key Management Scheme

There are two basic key management approaches, i.e., public and secret key-based schemes. The public key-based scheme uses a pair of public/private keys and an asymmetric algorithm such as RSA to establish session keys and authenticate nodes. In the latter scheme, a secret key is a symmetric key shared by two nodes, which is used to verify the data integrity. Although a public key management system can be fully self-organized, the initial trust among the nodes in a network is still built by using external mechanisms. For example, Capkun *et al.* propose such a system by constructing a local certificate repository (CR) for each node. The initial construction starts by issuing public key certificates based on a users' own knowledge about other users' public keys. Initially, there is a PKI or CA to distribute the knowledge among users. Therefore, the work is a dynamic maintenance mechanism in building up the certificates.

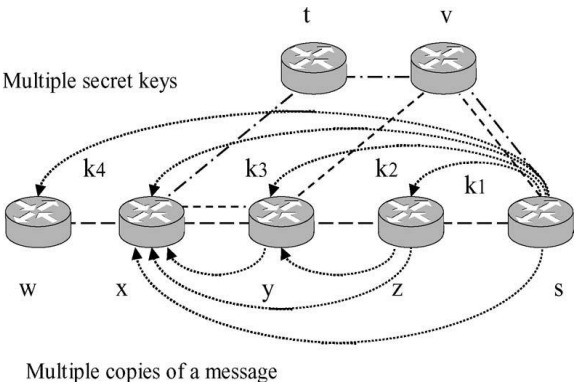

Fig.1 Demonstration of message and route redundancy.

Our framework for dynamic key management can be summarized as follows.

1) A secret key is established between the source and destination and some intermediate nodes along the route by using current public key information.

2) Each node along the route finds out which of its direct neighbors are faulty or compromised by using the established multiple keys between the source and intermediate nodes.

3) Each node updates its trustworthiness on each of its neighbors by using the observed node behavior and attack-detection results.

4) Each node constructs a local CR for the nodes it trusts. The certificates for those compromised nodes are immediately revoked. A node may expand its CR by adding newly trusted nodes or exchanging repository information with its trusted neighbors.

5) By combining the current CR information and existing maintenance procedures for public key management, the nodes in the network can update public key information or build up a self-organized PKI

Route Discovery and Attack Detection

Based on the key management mechanism, the next task is to develop a framework for the secure discovery of the dynamic network topology. The attack detection scheme is incorporated into topology discovery procedures. Route discovery is straightforward for a node after it decrypts the received route discovery messages. To discover the routes in a dynamic environment, we need to use the inherent redundancies of the routes in ad hoc networks, called *route redundancy*, which means there are multiple, possibly disjoint, routes between nodes. As long as there are sufficiently many correct nodes, the routing protocols should be able to discover routes that go around some compromised nodes. Many ad hoc routing protocols such as AODV and DSR can discover multiple routes. Similar methods can be adopted into our scheme to discover multiple routes.

To detect internal attacks, including Byzantine attacks, we assume the following.

1) Each node has a pair of public/private keys and a unique ID. A compromised node participates in routing until detected.

2) The source and destination nodes are secured by external security agents. There is a shared key between the source and destination nodes.

3) Each of the intermediate nodes between the source and destination has established a shared key with the source node by using the key management scheme.

4) There are enough uncompromised nodes in the network so that a message can arrive at the destination via different routes.

Routing Algorithm

The heuristic algorithm can be summarized as follows.

1) During route discovery, a source node sends RREQ packets to its neighboring nodes. In these packets, along with the regular information, the node also sends its securityrelated information, such as key information.

2) Once an RREQ packet is received by an intermediate node, it calculates the TQI. The node places the link trustworthiness and QoS information in the RREQ packet and forwards it to its next hop. This process is repeated until it reaches the final destination.

3) At the destination, the node waits for a fixed number of RREQs before it makes a decision. Or else, a particular time can be set for which the destination or intermediate node needs to wait before making a routing decision. Once the various RREQs are received, the destination node compares the various TQI index values and selects the index with the least cost. It, then, unicasts the RREP back to the source node. When the source node receives the RREP, it starts data communication by using the route.

4) Once the route is established, the intermediate nodes monitor the link status of the next hops in the active routes. Those that do not meet the performance and trustworthiness requirements will be eliminated from the route.

5) When a link breakage in an active route is detected, a route error (RERR) packet is used to notify the other nodes that the loss of that link has occurred. Some maintenance procedures are needed as in AODV.

Simulation Parameter

Mac type	mac/802-11
Number of nodes	30
Number of packets	60
Packet size	1500 Mb
Bandwidth	11Mb
Slot time	50microsec

Packet interval	0.020 equal to send rat 8000 bytes

Protocol

In this section we present a routing protocol with Byzantine robustness and detection. Byzantine robustness means that the protocol routes packets from source to destination as long as a non-faulty path exists. Byzantine detection means that the protocol identifies faulty links. We first give a definition of what constitutes a faulty component and then justify this definition.

A faulty node is a node that:

- does not follow our protocol, or
- can be impersonated by another node.

The first part of the definition captures a node that is controlled by an adversary or executes buggy code. The second part of the definition is not obvious: we associate the notion of faulty with that of malicious or harmful but in this case, the behavior of the faulty node does involve any malice. The faulty node can only be impersonated if, for example, its keys have been compromised. We cannot guarantee communication with a faulty node like this.

A faulty link is a link that:

- drops packets or
- is incident to a faulty node.

The first part of the definition is about links that have an impaired underlying communication system. Regarding the second part of the definition, we need to observe that a link that is incident to a faulty node can only route packets either from or to this node. If the faulty node has crashed, for example, then packets cannot be routed in either direction of the link. If the faulty node is a subverted one, then we would also like to avoid routing through this node, therefore identifying its incident links as faulty is equivalent from a routing robustness perspective to identifying this node as faulty. For performance reasons we would have liked to be

able to identify faulty routers. However, we cannot tell with certainty whether a link or the downstream router is faulty, although we do not preclude certain cases where this can happen. Another reason is that a faulty router can invalidate its incident link without provision from the protocol.

Therefore, if a link is detected to be faulty by our protocol, then one or more of the following statements are true:

- The upstream router is faulty.
- The underlying physical communication system is faulty.
- The downstream router is faulty.

The protocol can be seen as a combination of several components, each of which is important for the protocol's correctness. These components are:

1. source routing,
2. destination acknowledgements,
3. timeouts,
4. fault announcements,
5. authentication,
6. reserved buffers,
7. sequence numbers, and
8. FIFO scheduling.

Attacks:

Attacks Using Modification

An attacker node may modify certain contents of the routing packet, thus propagating incorrect information in the network. Attacker node may change Sequence number or hop count in AODV.

Attacks Using Impersonation

A malicious node may try to impersonate a node and send data on its behalf. This attack is generally used in combination with modification attack. An attacker node may cause routing loops by sending fake RREP advertising higher sequence number, causing neighboring nodes to falsely update their routing tables.

Packet Dropping

Black Hole

An attacker may create a routing black hole, in which all packets are dropped. by sending forged routing packets, the attacker could route all packets for some destination to itself and then discard them.

Gray Hole

As a special case of a black hole, an attacker could create a gray hole, in which it selectively drops some packets but not others, for example, forwarding routing packets but not data packets.

Byzantine Attacks

Byzantine attacks can be defined as attacks against routing protocols, in which two or more routers collude to drop, fabricate, modify, or misroute packets in an attempt to disrupt the routing services.

Network Simulator-2

NS-2 (Network simulator-2) is a discrete event simulator targeted at networking research. Ns provides substantial support for simulation of TCP, routing, and multicast protocols over wired and wireless (local and satellite) networks. Ns is based in two languages, an object oriented simulator written in C++ and an OTcl interpreter, used to execute user command scripts. NS has a rich library of network and protocol objects. There are two class hierarchies the compiled C++ hierarchy and interpreted OTcl one, with one to one correspondence between

them. The C++ compiled hierarchy allows us to achieve efficiency in the simulation and faster execution times. This is in particular useful for the detailed definition and operation of protocols. This allows one to reduce packet and even processing time. Then in the OTcl script provided by the user, we can define a particular network topology, the specific protocols and application that we wish to simulate and the form of the output that we wish to obtain from the simulator. The OTcl can make use of the objects complied in C++ though and OTcl linkage that create a matching OTcl object for each of the C++.

Simulation Results

Performance Evaluation

The performance metrics are defined as follows:

1. Packet delivery ratio (PDR): The ratio of the total number of data packets successfully delivered to the destination to the total number of data packets sent out by a source node.

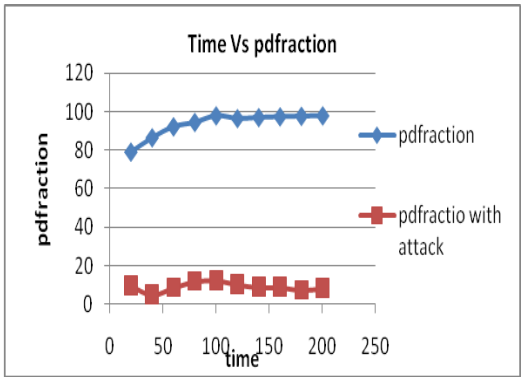

Fig.2 Pdfraction With and Without Attack

2. Average end to end delay: The average end-to-end delay of data packets is the interval between the data packet generation time and the time when the last bit arrives at the destination.

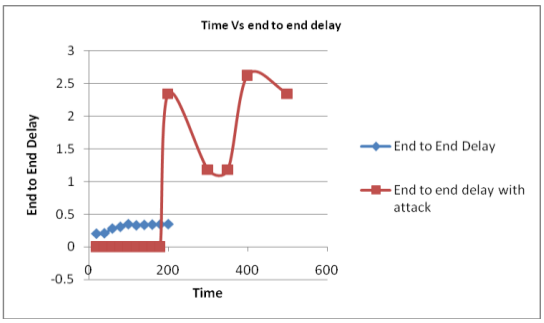

Fig.3 End to end delay With and Without Attack

3. Total throughput: The total number of data (application) packets that have been received at time *t* by a destination node.

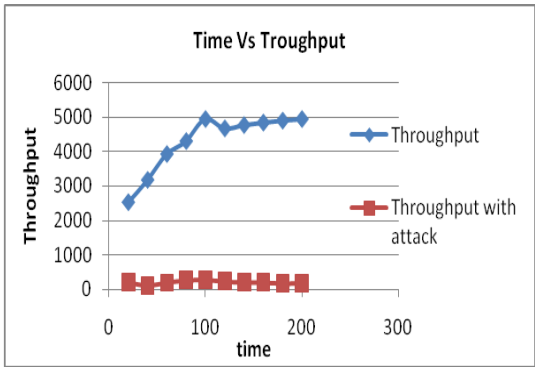

Fig.4 Troughput With and Without Attack

Conclusion

In this paper we implemented an AODV protocol that behaves as Black Hole in NS-2. We simulated five scenarios where each one has 20 nodes that use AODV protocol and also simulated the same scenarios after introducing one Black Hole Node into the network. Moreover, we also implemented a solution that attempted to reduce the Attack effects in NS-2. AODV network has normally 3.21 % data loss and if a Attack Node is introducing in this network data loss is increased to 92.59 %. As 3.21 % data loss already exists in this data traffic, Attack Node increases this data loss by 89.38 %.

Future Work

We simulated the Black Hole Attack in the Ad-hoc Networks and investigated its affects. In our study, we used the AODV routing protocol. But the other routing protocols could be simulated as well. All routing protocols are expected to present different results. Therefore, the best routing protocol for minimizing the Black Hole Attack may be determined. There are many Intrusion Detection Systems (IDS) for ad-hoc networks. These IDSs could be tested to determine which one is the best to detect the Black Hole.

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Experimental Investigations in a Circular Tube to Enhance Turbulent Heat Transfer Using Mesh Inserts

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Abstract

The present work focuses on experimental analysis of turbulent flow heat transfer enhancement in a horizontal circular tube by means of mesh inserts. Air is used as the working fluid. Sixteen types of mesh inserts are used with various screen diameters of 22 mm, 18 mm, 14 mm and 10 mm for varying distance between the screens of 50 mm, 100 mm, 150 mm and 200 mm. The horizontal tube was subjected to constant and uniform heat flux. The Reynolds number varied from 15,000 to 30,000. Initially the experiment was carried out without mesh inserts in the horizontal tube and then experiment is carried out using mesh inserts. Then both the results are compared for validation. An optimized relation is derived for both experimental and theoretical values. The optimized relation is derived on the basis of variation of heat transfer coefficient with diameter of mesh inserts and pitch between the mesh insertions.

Keywords: tube, heat transfer, mesh, turbulent flow, pressure drop, augmentation.

INTRODUCTION

In the recent years, considerable emphasis has been placed on the development of various augmented heat transfer surfaces and devices. This can be seen from the exponential increase in world technical literature published in heat transfer augmentation devices, rowing patents and hundreds of manufacturers offering products ranging from enhanced tubes to entire thermal systems incorporating enhancement technology. Energy and materials saving considerations, space considerations as well as economic incentives have led to the increased efforts aimed at producing more efficient heat exchanger equipment through the augmentation of heat transfer. Among many techniques investigated for augmentation of heat transfer rates inside circular tubes, a wide range of inserts have been utilized, particularly

when turbulent flow is considered. The inserts studied included twisted tape inserts, coil wire inserts, brush inserts, mesh inserts, strip inserts etc. The utilization of porous inserts has proved to be very promising in heat transfer augmentation. One of the important porous media characteristics is represented by an extensive contact surface between solid and fluid surfaces. The extensive contact surface enhances the internal heat exchange between the phases and consequently results in an increased thermal diffusivity. Different types of porous materials are extensively studied in forced convection heat transfer due to the wide range of potential engineering applications such as electronic cooling, drying processes, solid matrix heat exchangers, heat pipe, enhanced recovery of petroleum reservoirs etc. however the experimental work carried out in this area is limited.

Experimental studies conducted for heat transfer and pressure drop of laminar flow in horizontal tubes with/without longitudinal inserts (Shou-Shing Hsieh et al., 2003). They reported that enhancement of heat transfer as compared to a conventional bare tube at the same Reynolds number to be a factor of 16 at Re <= 4000, while a friction factor rise of only 4.5.

Hsieh and Kuo (Shou-Shing Hsieh et al., 2003) conducted experimental investigations for the augmentation of tube side heat transfer in a cross flow heat exchanger for turbulent flow of air by means of strip type inserts. They found that longitudinal strip inserts perform better than crossed strip (CS) and regularly interrupted strip (RIS) inserts for high Reynolds number (Shou-Shing Hsieh et al., 2003).

Hsiehand Wu (Shou-Shing Hsieh et al., 2000) conducted experimental studies on heat transfer and flow characteristics for turbulent flow of air in a horizontal circular tube with strip type inserts (longitudinal and Crossed Strip inserts). They reported that friction factor rise due to inclusion of inserts was typically between 1.1 and 1.5 from low Re (=6500) to high Re (=19500) with respect to bare tube. The experimental investigations of Hsieh and Liu (Shou-Shing Hsieh et al., 1996) report that Nusselt numbers were between four and two times the bare values at low Re an high Re respectively.

Bogdan I.Pavel (Bogdan I. Pavel et al., 2004) experimentally investigated the effect of

metallic porous inserts in a pipe subjected to constant and uniform heat flux at a Reynolds number range of 1000-4500. The maximum increase in the length-averaged Nu number of about 5.2 times in comparison with the clear flow case and a highest pressure drop of 64.8Pa were reported with a porous medium fully filling the pipe.

Devarakonda Angirasa, 2001 performed experiments that proved augmentation of heat transfer by using metallic fibrous materials with two different porosities namely 97% and 93%. The experiments were carried out for different Reynolds numbers (17,000-29,000) and power inputs (3.7 and 9.2 W). The improvement in the average Nusselt number was about 3-6 times in comparison with the case when no porous material was used.
Fu (Fu. H.L et al., 2001) experimentally demonstrated that a channel filled with high conductivity porous material subjected to oscillating flow is a new and effective method of cooling electronic devices.

Mehmet Sozen (Mehmet Sozen et al., 1996) numerically studied the enhanced heat transfer in round tubes filled with rolled copper mesh at Reynolds number range of 5000-19,000. With water as the energy transport fluid and the tube being subjected to uniform heat flux, they reported up to ten fold increase in heat transfer coefficient with brazed porous inserts relative to plain tube at the expense of highly increased pressure drop.

Paisarn Naphon (Paisarn Naphon et al., 2006) had experimentally investigated the heat transfer characteristics and the pressure drop in horizontal double pipes with twisted tape insert. The results obtained from the tube with twisted insert are compared with those with out twisted tape.

Liao. Q (Liao. Q et al., 2001) carried out experiments to study the heat transfer and friction characteristics for water, ethylene glycol and ISOVG46 turbine oil flowing inside four tubes with three dimensional internal extended surfaces and copper continuous or segmented twisted tape inserts within Prandtl number range from 5.5 to 590 and Reynolds numbers from 80 to 50,000. They found that for laminar flow of VG46 turbine oil, the average Stanton number could be enhanced up to 5.8times with friction factor increase of 6.5fold compared to plain tube.

Betul Ayhan Sarac (Betul Ayhan Sarac et al., 2007) conducted experiments to investigate heat transfer and pressure drop characteristics of a decaying swirl flow by the insertion of vortex generators in a horizontal pipe at Reynolds numbers ranging from 5000 to 30000. They observed that the Nusselt number increases ranging from 18% to 163% compared to smooth pipe. Experimental investigation on heat transfer and friction factor characteristics of circular tube fitted with right-left helical screw inserts of equal length and unequal length of different twist ratios was done by (Sivashanmugam, et al., 2007). They observed that heat transfer coefficient enhancement for right left helical screw inserts is higher than that for straight helical twist for a given twist ratio. A maximum performance ratio of 2.97 was obtained by helical screw inserts. Heat transfer, friction factor and enhancement efficiency characteristics in a circular tube fitted with conical ring turbulators and a twisted-tape swirl generator were investigated experimentally by Promvonge (Promvonge, et al., 2007). Air was used as test fluid. Reynolds number varied from 6000 to 26000. The average heat transfer rates from using both the conical-ring and twisted tape for twist ratios 3.75 and 7.5, respectively are found to be 367% and 350% over the plain tube.The effect of two tube insert wire coil and wire mesh on the heat transfer enhancement, pressure drop and mineral salts fouling mitigation in tube of a heat exchanger were investigated experimentally (Pahlavanzadeh H. et al., 2007) with water as working fluid. The heat transfer rate averagely increased by 22-28% for wire coil and 163 -174% for wire mesh over a plain tube value depending on the type of tube insert, density of wire torsion and flow velocity. Pressure drop also increased substantially by 46% for wire coil and 500% for wire mesh. As Bogdan I. Pavel (Bogdan I. Pavel *et al*., 2004) carried out their work in a pipe with porous inserts in laminar and turbulent region with Reynolds number ranging from 1000-4500, the present work has been done similar lines but in turbulent region (Re number range of 7,000-14,000) as most of the flow problems in industrial heat exchangers involve turbulent flow region.

EXPERIMENTAL PROCEDURE

The apparatus consists of a blower unit fitted with a pipe in horizontal orientation. Nichrome bend heater encloses the test section to a length of a 40cm. Four thermocouples are embedded on the walls of the tube and two thermocouples are placed in the air stream, one at

the entrance and the other at the exit of the test section to measure the temperature of flowing air shown in Figure-1.

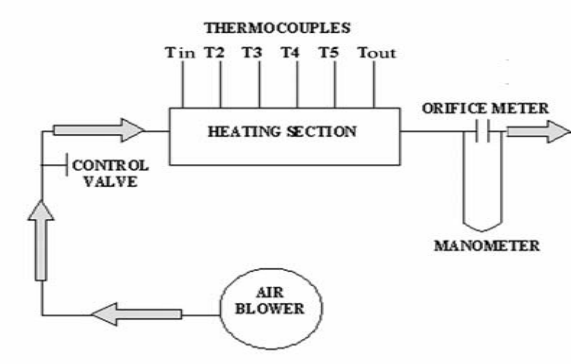


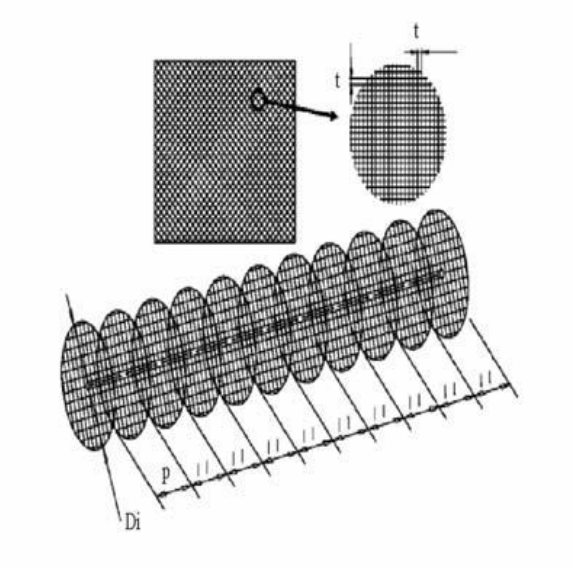
Figure-1. Experimental Setup.

The test pipe is connected with an orifice to measure the flow of air through the pipe. Input to heater is given through dimmer stat. The velocity of airflow in the tube is measured with the help of orifice plate and the water manometer fitted on the board. The inner tube of the heating part which is the test tube with inside diameter 27.5mm is made of 3.2 mm thick copper plate. A heat generating element is wound around this test tube so that the required heat input is given. The thermocouples (J-type) with accuracy ±0.4% are installed and drilled into the backside of the tube wall. Display unit consists of voltmeter, ammeter, dimmer stat and temperature indicator. Heat input can be varied by changing the voltage and current which are in turn altered by the dimmer stat position. The circuit was designed for a load voltage of 0-220 V, with a maximum current of 10 A. Outlet of the test pipe section is connected to an orifice meter and a manometer so that the pressure drop, mass flow rate of air can be measured.

The fluid properties were calculated as the average between the inlet and the outlet bulk temperature. It took 90mins to reach steady state conditions. Experiment was carried out at constant heat flux conditions and constant heat input of 40 W at different mass flow rates, with and without the inserts. In this, we assume that the air flowing through the circular tube to be hydro dynamically and thermally fully developed turbulent flow.

The porous media used for the experiments are Copper screens (wire diameter 0.28 mm) cut out at various diameters (D_i) and then inserted on copper rods as shown in Figure-2.

That is, 16 different inserts were obtained by varying the screen diameter and the distance between two adjacent screens (p). Due to insertion of the mesh inserts the hydraulic diameter reduces and the velocity in the pipe increases resulting in enhanced heat dissipation from the heating section.



SEQUENCE OF OPERATIONS

Experiments are carried out first without inserts and then with inserts.

Without inserts

Initially the experiment is carried out without any insert. The working fluid air flows through the pipe section with least resistance.

With inserts

In this, the mesh inserts with different diameters and pitches are taken as shown in Table-1. The mass flow rates considered for the constant heat input of 40 W in terms of water level difference in U-Tube water manometer are 2 inch, 3 inch, 4 inch and 5 inches(0.0047 to 0.0055(Kg/sec) of air).

PROCEDURE TO INSERT THE INSERTS

Photographic view of the inserts is shown in Figure-3. Each insert is taken and inserted into the test section axially. It is taken care that the strip doesn't scratch the inner

wall of the pipe and get deformed. The presence of the insert in the pipe causes resistance to flow and increases turbulence.

Mesh Diameter (D_i)	**Pitch** (p)
22mm	50mm
18mm	100mm
14mm	150mm
10mm	200mm

Table-1. Shows the Mesh insert diameters along with different pitches.

2.4 Heat Transfer Calculations

$T_s = (T2+T3+T4+T5)/4$ (1)

$T_b = (T1+T6)/2$ (2)

Discharge of air,

$$d=C_d \sqrt{2gh(\rho m - \rho a)} \Big/ \sqrt{\rho a(1-\beta)} \quad (3)$$

Velocity of air,

$$V_a = (Vo * Ao) / A \quad (4)$$

Reynolds number, Re=U D/□ (5)

(To calculate Re while using mesh inserts, Dh instead of D is used)

Wetted perimeter= ∏.(Di+D) (6)

Dh= 4g.(A_{fr} /Wetted perimeter)) (7)

Q =m.Cp.(T1-T6) (8)

h = Q/(A (Ts - Tb)) (9)

Nu = hD/K (12) (10)

Table 2: Mesh insert diameters along with different pitches.

Mesh insert Number	Diameter	Pitch	Rp
1	22	50	0.8
2	22	100	0.8
3	22	150	0.8
4	22	200	0.8
5	18	50	0.65
6	18	100	0.65
7	18	150	0.65
8	18	200	0.65
9	14	50	0.5
10	14	100	0.5
11	14	150	0.5
12	14	200	0.5
13	10	50	0.34
14	10	100	0.34
15	10	150	0.34
16	10	200	0.34

Table 3: Experimental and Theoretical values of heat transfer coefficient and Nusselt number for mesh diameter 22mm with various pitch values

Pitch (mm)	Experimental		Theoretical	
	H	Nu	H	Nu
50	155.09	91.33	253.42	ss149.23
100	153.09	90.87	241.72	143.41
150	150.07	89.64	239.51	142.49
200	148.57	88.58	236.17	140.82

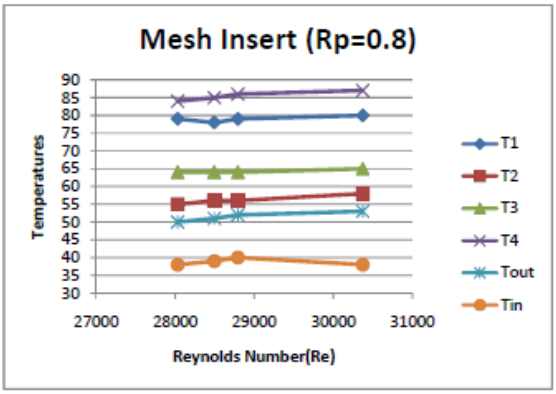
Table 4: Experimental and Theoretical values of heat transfer coefficient and Nusselt number for mesh diameter 18mm with various pitch values.

Pitch (mm)	Experimental		Theoretical	
	H	Nu	h	Nu
50	146	91.28	228.09	143
100	144.24	90.61	222.08	139.71
150	141.49	89.38	219.15	138.44
200	140.89	89.11	210.49	133.14

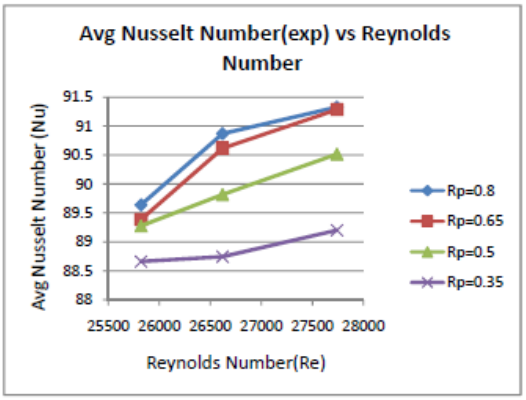
Results and discussions

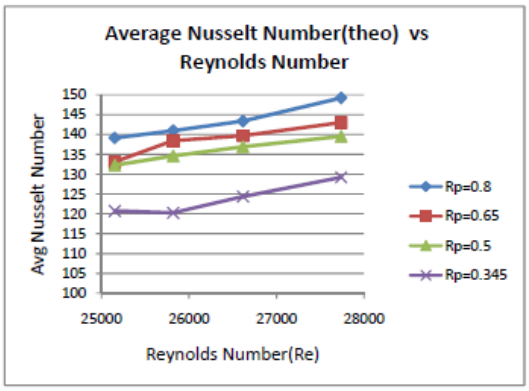
Experimentally determined Nusselt number values for plain tube (without mesh insert) are compared with Dittus-Boelter correlation.

Figure 2.0 shows the variation of surface temperature with Reynolds number for mesh insert of diameter 22mm. As the mesh is inserted into the horizontal tube of test section diameter 28mm turbulence is created thereby increasing the surface temperature.

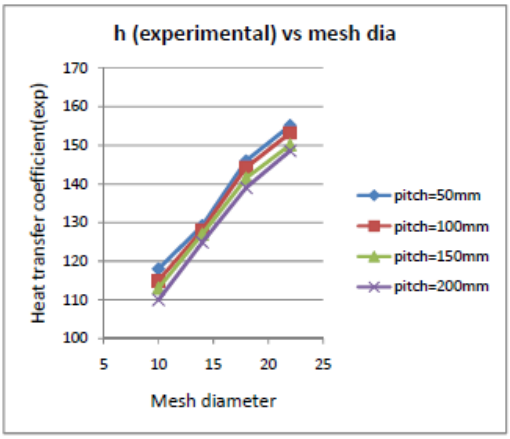


The variation of surface temperature with Reynolds number for mesh insert of diameter 18mm. As the diameter of mesh insert is reduced from 22mm to 18mm and inserted into the horizontal tube of test section diameter 28mm, the turbulence which is created in the tube reduced there by reducing the surface temperatures.

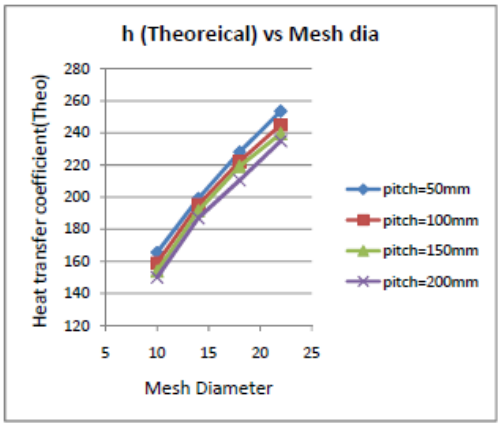




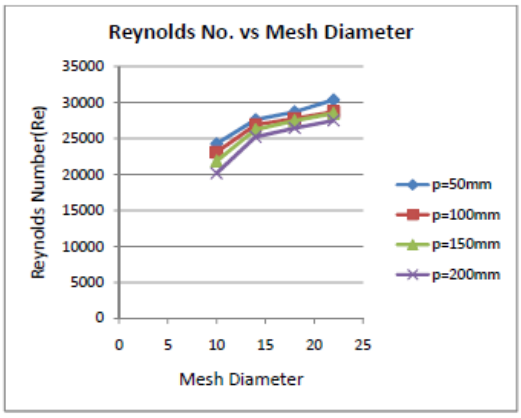
Our present work main objective is to enhance the heat transfer by inserting mesh inserts into the horizontal tube of test section diameter 28mm. Figure 2.6 shows the variation of experimental heat transfer coefficient with mesh diameter for different values of pitch. From the figure it is observed that the mesh diameter of 22mm with pitch of 50mm yields the highest experimental heat transfer coefficient value when compared to the rest of mesh inserts. Figure 2.7 shows the variation of theoretical heat transfer coefficient with mesh diameter for different values of pitch. From the figure it is observed that the mesh diameter of 22mm with pitch of 50mm yields the highest theoretical heat transfer coefficient value when compared to the rest of mesh inserts.



The variation of theoretical heat transfer coefficient with pitch for different values of mesh diameters. From the figure it is observed that the mesh diameter of 22mm with pitch of 50mm yields the highest theoretical heat transfer coefficient value when compared to the rest of mesh inserts.



The variation of Reynolds number with pitch for different mesh inserts. From the figure it is observed that the mesh diameter of 22mm with pitch of 50mm yields the highest Reynolds number when compared to the rest of mesh inserts.



From the above all discussions it is found that experimental and theoretical value of heat transfer coefficient is varying with mesh diameter and pitch. When the meshes are inserted into the horizontal tube hydraulic diameter is considered instead of mesh diameter. Hence heat transfer coefficient is varying with hydraulic diameter. Finally an optimized relation is derived in both experimental and theoretical cases.

Experimental Case

h = 54.9705 (d) 0.42247 (p)-0.05899

From the above relation heat transfer coefficient is directly proportional to mesh diameter and inversely proportional to pitch.

h = 6274.8 (dh)-1.221 (p)-0.0609

From the above relation heat transfer coefficient is inversely proportional to hydraulic diameter and pitch.

Theoretical Case

h = 55.7442 (d) 0.5503 (p)-0.0469

From the above relation heat transfer coefficient is directly proportional to mesh diameter and inversely proportional to pitch.

h = 26173.39 (dh)-1.5839 (p)-0.04942

From the above relation heat transfer coefficient is inversely proportional to hydraulic diameter and pitch.

Conclusion

Heat transfer coefficient depends on the parameters-mesh diameter, hydraulic diameter and pitch. When we consider Mesh diameter the relation with heat transfer coefficient is directly proportional to mesh diameter and is inversely proportional to pitch. When we consider Hydraulic diameter the relation with heat transfer coefficient is inversely proportional to mesh diameter and pitch. As mesh diameter increases Reynolds number and velocity of air increases. As hydraulic diameter increases Reynolds number and velocity of air increase. As pitch increases Reynolds number and velocity of air decreases. Effective heat transfer coefficient value is obtained at 22mm mesh diameter and 16.6mm hydraulic diameter with 50mm pitch value.

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An Experimental Study on the Influence of Machining Parameters When Machining Tool Steel Using Die-Sinking EDM

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Abstract

Copper tungsten electrode of 14 mm diameter was used in electrical discharge machining (EDM) of P 20 tool steel at different current, pulse-on time and pulse-off time settings with the objective of determining possible correlation between EDM parameters and the machinability factors. Experiments were conducted using Taguchi method. Each test was performed for 15 mins and EDF-K diamond oil was used as the dielectric fluid. The material removal rate of the workpiece was obtained based on the calculation of mass loss per machining time and surface roughness was obtained based on the average of readings. It was found that material removal rate as well as surface roughness was dependent on peak current, pulse-on time and pulse-off time. High peak current, low pulse-on time and high pulse-off time was found suitable for minimum surface roughness. High peak current, high pulse-on time and low pulse-off time was found suitable for maximum material removal rate.

Keywords: Sinking EDM, Peak current, Pulse-on time, Pulse-off time, Taguchi method, Material removal rate, Surface roughness

I INTRODUCTION

Recently, many researchers have done their work in the field of electrical discharge machining by machining various combinations of workpieces and tool materials in order to reduce the wear of electrode and to increase the material removal rate in the workpiece [3]. From the researches, it is observed that by manufacturing composite electrode, it is possible to reduce

wear and to increase the material removal rate. In this paper, it is decided to use copper tungsten electrode and P20 tool steel [11] to find the maximum material removal rate and minimum surface roughness. EDM is successfully used in the field of tool and die making. Pure electrode materials find considerable advantage in the EDM process because of their electrical conductivity. But wear in those electrodes will be more.

Hence, to reduce the wear electrodes are being manufactured in polymer, composite materials and in alloy materials like copper tungsten, silver tungsten. But copper tungsten electrode is economical compared to other alloy electrodes and is being used in the industries world wide. Hence, as wear is less in copper tungsten [1] electrodes this study is focused on material removal rate and surface roughness in workpiece when machining tool steel using copper tungsten electrode.

II EXPERIMENTAL DETAILS

A. *Working principle of EDM*

EDM is the non-conventional method of machining the workpiece using current as a tool. This method is used to cut very hardened workpieces of HRC 62 or more(any hardness). Dielectric oil such as Diamond EDF K oil is used to decrease the arc area so that uniform machining takes place. Machining parameters such as pulse-on time, pulse-off time, gap current [2] should be carefully controlled to obtain precise machining. Hence it is necessary to choose optimum electrode material which provide better surface finish. Polarity of the electrode, servo voltage, gap, machining time, gain are kept constant in this experiment

The electrode was clamped in the electrode holder which has capacity to hold 25 Kg of electrode weight. The workpiece was kept on the machine table and the electrode surface was made to touch the workpiece ground surface. The centre of the workpiece was measured by measuring four sides of rectangular workpiece by setting the work coordinates. Depth was set using Z axis on the machine. Immediately the beep sound was heard, flushing should be

switched on. The machine is ready for machining. For this application depth of 1 mm was selected and machining time was set as 15 mins [4].

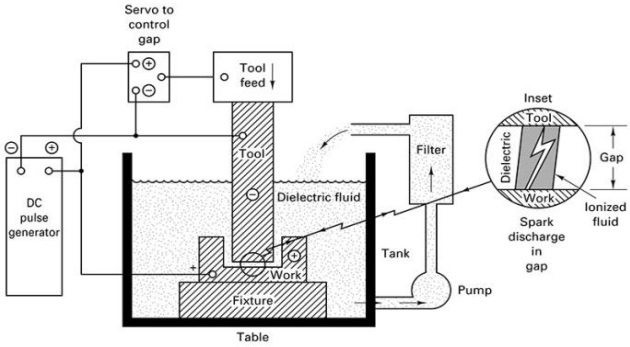

Fig. 1. EDM Process Diagram

The suitable combinations of input parameters such as peak current, pulse-on time and pulse-off time produce stationary MRR and surface roughness.

Moreover the anode melts faster than the cathode due to the absorption of fast moving electrons at the starty of pulse, then begins to resolidify after few micro seconds. The process creates small craters on the material surface, their size and shape depends on the discharge of the energy (as well as the pulse shapes), electrode material thermal properties and heat conduction pattern.

B. *Specifications of the machine*

- Machine : Mitsubishi CNC EDM
- Axis stroke : 300 x 250 x 250 mm
- Workpiece : 740 mm x 470 mm x 150 mm
- Max. electrode weight : 25 Kg
- Max. workpiece weight : 550 Kg
- EDM Oil : Diamond EDF-K

From the above specifications and based on the weight measurements workpiece size of 28 x 27 x 8 mm is chosen and 14 mm electrode is chosen. In this study two assumptions were made:

(a) EDM oil temperature and pressure was maintained as constant throughout the experiment (b) Voltage was assumed to be constant [4].

C. *Workpiece and Electrode material*

- Workpiece size : 28 x 27 x 8 mm
- Material : P20 Toolsteel
- Composition : 40crMnNiMo864
- Electrode size : 14 mm
- Depth of cut : 1 mm
- Electrode material : Cu-W (30 % - 70 %)
- Flushing : Emission flushing

In order to have less electrode wear, better surface roughness and higher machining rates it was proposed to use copper tungsten electrode of above combination. The dielectric fluid has four main functions electrical insulation, spark conductor, flushing medium and coolant. Since, flushing plays the main role in EDM emission flushing in which the coolant (or) dielectric will point in the inter electrode gap so that the spherical debris will be removed with ease.

D. *Material removal rate (MRR)*

Material removal rate is related to the amount of mass loss [4] in work piece after machining 15 minutes in EDM machine. In EDM, material removal rate increases with increase in the peak current and pulse-on time which leaves rough surface quality. Researches are going on in EDM machine to increase machining speed and to reduce surface roughness value. Higher amounts of material removal rate settings can be best utilized in rough machining conditions. Material removal rate can be increased by increasing di-electric flushing pressure and different combinations of parameter settings. MRR can be improved by delivering additional discharges using multiple electrodes. MRR can be improved using tubular electrodes in which air is supplied in the centre micro holes of the electrode. The simultaneous rotation of the electrode with air removes lot of material and can be used very well for rough machining conditions. This

experiment focuses on highest material removal rate with less surface roughness with 25 no. of possible experiments.

Hence, material removal rate increases with increased peak current, pulse-on time, flushing pressure, no. of holes in the electrode, by increasing no. of electrodes and by attaching additional mechanism for contouring.

E. *Surface roughness*

This project is focused on lesser surface roughness by setting the lower pulse-off time and higher (or) lower current and less dielectric flushing pressure. Surface roughness decreases with higher pulse-off time and less peak current. In order to achieve the minimum surface roughness, it is necessary to reduce the pulse-on time, increase the pulse-off time, increase (or) decrease the peak current according to the pulse-off time setting with super finished electrode.

III PROBLEM DEFINITION

As seen from the literature surveys, researchers have found techniques to detect electrode wear and material removal rate using conventional electrode materials such as copper and graphite and have done researches on large number of tool steels (DC 53, P20, Ceramics etc.). In this study, EDM machining of AISI P20 material using copper tungsten composite electrode will be carried out and the responses such as material removal rate, surface roughness and tool wear rate will be discussed in detail.

During the machining of conductive materials, electrode wear occurs due to which electrode losses it's shape and consequently, workpiece cannot be machined to a specific shape mentioned in the drawing which is the problem frequently encountered in electrodes like copper, graphite. In this experiment one electrode is used from rough to finish machining stages in order to predict tool wear. Tungsten is blended with copper in order to resist wear which is used to machine P20 toolsteel used in many mold industries.

IV OBJECTIVES

1. Machining the workpieces for each trial of experiment.
2. Measurement of material removal rate and surface roughness for the experiments.
3. Validation of results with ANOVA and Genetic algorithm using matlab.

V DESIGN OF EXPERIMENTS

A. *Orthogonal array*

The selection of orthogonal array to use predominantly depends on number of factors and interactions of interest, number of levels for the factors of interest, desired experimental resolution and cost limitations. The first two items determine the smallest orthogonal array which is possible to use.

B. *Array selection*

There are two basic kinds of orthogonal arrays which are two level arrays (L4, L8, L12, L16, L32) and three level arrays (L9, L18, L27). The number in the array designation indicates the number of trials in the array. An L8 has eight trials and an L27 has 27 trials. The number of levels used in the factors should be used to select either two-level or three level types of orthogonal arrays. Orthogonal array selection should also be made using degrees of freedom for main factors and for interactions. This strategy will minimize the total number of tests to be conducted yet will yield meaningful information at the same time. Once, the appropriate orthogonal array has been selected, the factors can be assigned to various columns of the array and subsequent interaction columns located [20].

C. *Degrees of freedom*

A degree of freedom in a statistical sense is associated with each piece of information that is estimated from the data. Degree of freedom is one of the main criteria in deciding orthogonal arrays. In this project, main effects of factors are considered and for each factor, degree of freedom is number of levels for each factor minus one. Hence, using the above criteria for selection of orthogonal arrays, in this project 12 degrees of freedom arrived and for the above

degrees of freedom, L25 orthogonal array is selected in order to have higher resolution. Another criterion in deciding orthogonal array for the experiment is number of runs should be greater than or equal to chosen degrees of freedom.

D. *L 25 Orthogonal array*

The design which was finally chosen was L 25 orthogonal array due to higher amount of resolution. This orthogonal matrix has 6 columns which can be used for input parameters. Basically this orthogonal array is designated as L 25 (5^6). For this experimentation work first three columns have been chosen.

Table 1

Factors and levels selected for the experiment

		Levels				
Sl. No	**Parameters**	**1**	**2**	**3**	**4**	**5**
1	Peak current, **I_p(A)**	0.2	1.2	2.2	3.2	4.2
2	Pulse-on time, **t_{on} (µs)**	2.6	3.6	4.6	5.6	6.6
3	Pulse-off time, **t_{off} (µs)**	4.2	5.2	6.2	7.2	8.2

Table 1 presents the relationship between the design factors and their corresponding selected variation levels taking into account that the study wanted to focus on material removal rate and surface roughness.

Table 2

Design of experiment matrix

Runs	I_p(A)	t_{on} (µs)	t_{off} (µs)
1	1	1	1
2	1	2	2
3	1	3	3
4	1	4	4
5	1	5	5
6	2	1	2
7	2	2	3
8	2	3	4
9	2	4	5
10	2	5	1
11	3	1	3
12	3	2	4
13	3	3	5
14	3	4	1
15	3	5	2
16	4	1	4
17	4	2	5
18	4	3	1
19	4	4	2
20	4	5	3
21	5	1	5
22	5	2	1
23	5	3	2
24	5	4	3

25	5	5	4

Runs	Material removal rate (g/min.)	S/N ratio for MRR
1	1.20×10^{-3}	-58.416
2	6.0×10^{-4}	-64.437
3	1.23×10^{-3}	-58.202

Table 2 shows the design matrix resulting from the type of experiment selected. The importance of the input parameters in the EDM process was determined. The possible influential machining parameters were selected according to literature review. There are three input parameters that affect the EDM performance. Some of these parameters are likely to have a more significant effect on electrical discharge machining performance than others. The levels of input parameters were selected considering rough cut and finish cut conditions.

VI RESULTS AND DISCUSSION

A. *Material removal rate (MRR) results*

Table 3

Material removal rate results

4	2.0×10^{-4}	-73.979
5	4.666×10^{-4}	-66.621
6	1.333×10^{-4}	-77.503
7	1.466×10^{-3}	-56.677
8	1.533×10^{-3}	-56.289
9	6.666×10^{-4}	-63.523
10	1.666×10^{-3}	-55.567
11	2.20×10^{-3}	-53.152
12	1.466×10^{-3}	-56.677
13	1.466×10^{-3}	-56.677
14	0.02746	-31.226
15	0.02333	-32.642
16	4.133×10^{-3}	-47.675
17	3.4×10^{-3}	-49.370
18	0.0622	-24.124
19	0.0566	-24.944
20	0.0559	-25.052
21	1.4×10^{-3}	-57.077
22	0.0698	-23.123
23	0.0699	-23.111
24	0.0754	-22.453
25	0.0750	-22.499

Table 3 presents the results for material removal rate and signal to noise ratio. Material removal rate was calculated by subtracting weight of workpiece before and after machining for 15 mins. From the above table, it is clearly seen that for runs 14, 15, 18, 19, 20, 22, 23, 24, 25 signal to noise ratio had increased compared to other runs.

B. *Analysis of material removal rate*

Table 4

ANOVA table for material removal rate

Source	DF	Seq SS	Adj SS	Adj MS	F	P
I_p	4	4936.2	4936.2	1234.04	29.94	0.000
T_{on}	4	1076.5	1076.5	269.12	6.53	0.005
T_{off}	4	1243.8	1243.8	310.95	7.54	0.003
Residual Error	12	494.6	494.6	41.22		
Total	24	7751.0				

Table 4 clearly shows that P value for peak current and Pulse-off time are in higher influence than Pulse-on time and hence is considered as the most influential parameter in the experimentation process and higher the peak current, higher the material removal rate. The regression equation for material removal rate is obtained and is given by

$$MRR = 0.0005 + 0.0150\ I_p + 0.00756\ t_{on} - 0.00756\ t_{off} \quad \ldots\ldots (1)$$

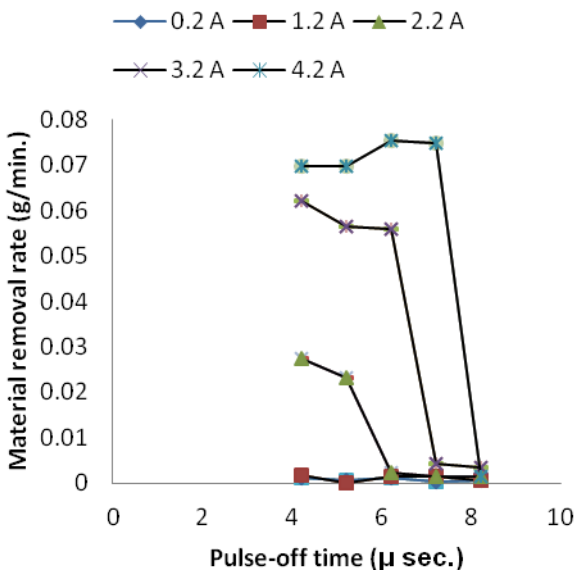

Fig . 2. Material removal rate Vs Pulse-off time

Fig. 2 clearly shows the relation between material removal rate and pulse-off time at different current settings (0.2 A, 1.2 A, 2.2 A, 3.2 A, 4.2 A) and it is clearly seen that at 4.2 µ sec. material removal rate is higher. Since, 4.2 µ sec. is the first level of pulse-off time, peak current and pulse-on time dominates and the material removal rate is increased. The material removal rate starts decreasing at higher levels of pulse-off time and surface roughness at higher levels of pulse-off time is lesser.

VII CONCLUSION

The experimental study of the EDM of AISI P20 tool steel provided important quantitative results for obtaining machining outputs as follows:

a. Material removal rate increases with increased peak current (I_p) and decreased pulse-off time (t_{off}).

b. From ANOVA table, it is found that peak current and pulse-off time are the most influencing parameters for EDMing P20 tool steel with copper tungsten electrodes.

c. From the graph of material removal rate versus pulse-off time, it is found that for lesser pulse-off time in all current settings material removal rate is higher.

d. Since, lesser pulse-off time reduces the time for dielectric flushing in the inter electrode gap (IEG), material removal rate is higher.

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Human Identification Using FKP, IRIS and FV Images

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Abstract

Biometric Recognition will provide strong link between individual and claimed identity. In modern years, biometrics is largely used for personal recognition. In this paper, a new combined biometric system, namely, Finger-Knuckle-Print (FKP), Finger vein and IRIS, is proposed. We can extract the FKPs features by Linear Discriminate Analysis (LDA), and Finger Vein and IRIS features by the 2D Block based on Gabor method. Finally, performance of all finger knuckle, vein and iris are determined individually and a min rule fusion is applied to develop a combined authentication system. Experimental results show that LDA is the best performance for identifying FKPs, and Gabor is the best performance for IRIS as well as Finger vein and it is able to provide an excellent recognition rate and more security.

Keywords*:* Finger Knuckle Print, IRIS, LDA, Finger Vein, Gabor, Recognition.

I. INTRODUCTION

Biometrics is used to identify a person using one's physiological or characteristics Human physiological and/or behavioural characteristic can be used as a biometric feature when it satisfies the requirements as ubiquity, peculiarity, stability and collectability. Well known Biometric features are fingerprints, hand veins, handwritten signatures, retinal patterns, ear patterns, etc. Hand-based biometrics has been fascinating considerable attention over present years due to its ease in accession.

Presently, it is noticed that the dorsum of hand has the potential to do personal authentication. The texture pattern is captured by bending the finger knuckle of a person, and it is hugely unique and thus can serve as a distinct biometric feature. The user acceptance for the outer finger surface imaging can be very huge as, unlike attractive fingerprints, there is no stigma of criminal examination associated with finger knuckle surface imaging [2]. The peg-free imaging of the finger knuckle surface is hugely convenient to users and offers very huge potential for reliable personal identification and authentication. The appearance

based approach examination in for the finger knuckle identification cannot exploit line based features and therefore achieves quality performance. The finger knuckle surface is hugely rich in lines and creases, which are fairly curved but hugely unique for individuals.

Compared to fingerprint, iris are stable and fixed throughout life.

II. RELATED WORK

A survey of identification and authentication using finger knuckle, finger vein and iris surface are described below. The finger knuckle bending is hugely unique biometric identifier. Similarly finger vein patterns are unique, even in identical twins. Finger veins are hidden structure and its difficult to steal without their knowledge. It also offers strong antispoofing and it ensures liveness in the presented fingers during imaging.

Iris recognition is one of the most important biometric technologies due to its accurate and reliable advantages Iris localization means, it calculates the positions of iris boundaries, and extracts the iris region in iris recognition [7]. Our classical iris localization method is shown below.

$$\max(r, x_0, y_0) \left| G_\sigma(r) * \frac{\partial}{\partial r} \frac{I(x, y)}{2\pi r} ds \right|_{r, x_0, y_0} \quad (1)$$

Where * denotes convolution and $G_\clubsuit(r)$ is a smoothing function. The method searches on the three dimensional space (r, x_0, y_0), takes a long time to complete the localization. Gabor method presents a robust, real-time algorithm for localizing the iris of an eye image. It localizes the outer boundary of the iris first and then localizes the inner boundary. The method consumes huge computational cost. Finally all biometric recognition methods are integrated to improve the performance.

III. ARCHITECTURE AND MODELING

Having the database of FKP images of all the people consumes more space and complexity. So, here we use user identification number (UID) for each person. The FKP image features as number of peaks in

the Gabor Wavelet graph and the successive distances between those peaks are stored in the database corresponding to particular UID. During authentication, the person has to hand over the UID and his FKP image is captured. If the features of new captured image match with the corresponding features in the database would mean then the person will be authenticated [11].

A. *FKP Image Acquisition*

A specially get FKP image acquisition databases are get from PolyU FKP Database[1].

B. *Pre-processing*

Captured image is converted into gray-scale format. Then the region of interest (ROI) is extracted from FKP image. The original FKP image and the corresponding ROI FKP image is shown in Figure 1(a) and 1(b) properly. The edges are detected by local maxima of the gradient of image. Gaussian filter is used to calculate The gradient of an image $f(x, y)$ and its defined as

$$G_x = \frac{\partial f}{\partial x} \quad (2)$$

$$\nabla f \quad \square \quad \square$$

$$G_y \quad \frac{\partial f}{\partial y}$$

The magnitude ∇f is given as,

$$\nabla f \quad \square \quad mag\square\nabla f \square \square \square G_x^2 \quad \square \quad G_y^2 \quad \square^{1} \quad (3)$$

To detect strong and weak edges we can use two thresholds. Fig. 2 shows the image after edge

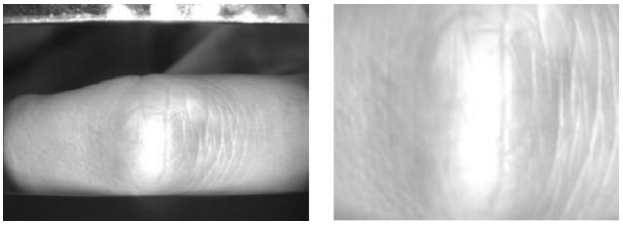
detection. The algorithm for edge detection is given in Table I. Algorithm uses Median filter, which is given as –

$$\hat{f}(x,y) = \underset{(s,t)\in S_{xy}}{median}\{g(s,t)\} \quad (4)$$

Here, S_{xy} represents the set of coordinates

C. Feature Extraction

The features are extracted using Gabor Wavelet transform. It has two components real and imaginary and can be convolved with an image to estimate the magnitude of wavelength and orientation in the image[2].



(a) Original FKP Image (b) Extracted ROI

Fig. 1 Test Image 1

Fig. 2 Phase Congruency and LDA for Test Image1

TABLE I

1. The input image is smoothed using a Gaussian filter (specified standard deviation σ), to reduce noise. 2. Determine The local gradient, $g(x, y) = \sqrt{G_x^2 + G_y^2}$, and edge point $\frac{G_x}{G_y}$ 3. Consider two thresholds T1 and T2.Pixels with values greater than T2 are said to be strong edge pixels. Other Pixels are said to be weak edge pixels.

By applying Gabor wavelet, we will get resultant image as shown in Figure 3.

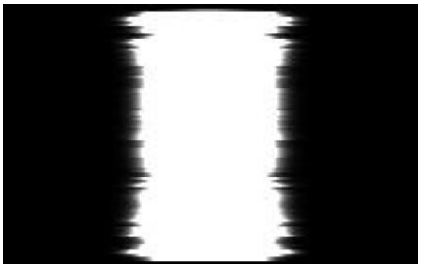


Fig. 3 Gabor Image obtained for Test Image1

D. Feature Matching

Now we have two sets of values containing peak-points – a set, *A* image is from the database for a particular person, and set *B* is of input FKP image of a person waiting to get authenticated. Now, compute the consecutive distance between the points in *A* as –

$$d_{Ai} = \sqrt{(x_{Ai} - x_{A(i+1)})^2 + (y_{Ai} - y_{A(i+1)})^2} \quad (5)$$

Here, $i = 1 \ldots M - 1$. Similarly, the successive distances between the points in *B* are –

$$d_{Bj} = \sqrt{(x_{Bj} - x_{B(j+1)})^2 + (y_{Bj} - y_{B(j+1)})^2} \quad (6)$$

Based on the above result we get a sequence of successes and failures. Probability of success as –

$$P = \frac{\text{the number of success observed}}{S_{count}} \quad (7)$$

total number of comparisons made $\overline{n}$

The probability always ranges from 0 to 1 indicating no chance to 100% chance. If the computed value of P is greater than 0.60 (a threshold value), then we can decide the person is authenticated or not.

E. Iris Recognition

Iris Recognition consists of three modules: image pre-processing, feature extraction, and authentication modules. Since the system is tested on the UBIRIS iris image database [8].

1. Pre-processing Module

Input image has useless data derived from the surrounding eye region. Image must be pre-processed like localize, segment and enhance the region of interest. Image pre-processing module has three units: iris localization, iris segmentation with coordinate transform, and enhancement units, as shown in Fig. 4.

2) Iris Localization Unit

The iris is an annular region between the pupil and the sclera. Iris localization unit performs an operation of enhancing principal edges and blurring useless edges on the copied and down sample image instead of the original one. Following that, the system estimates the centre coordinates of the iris first.

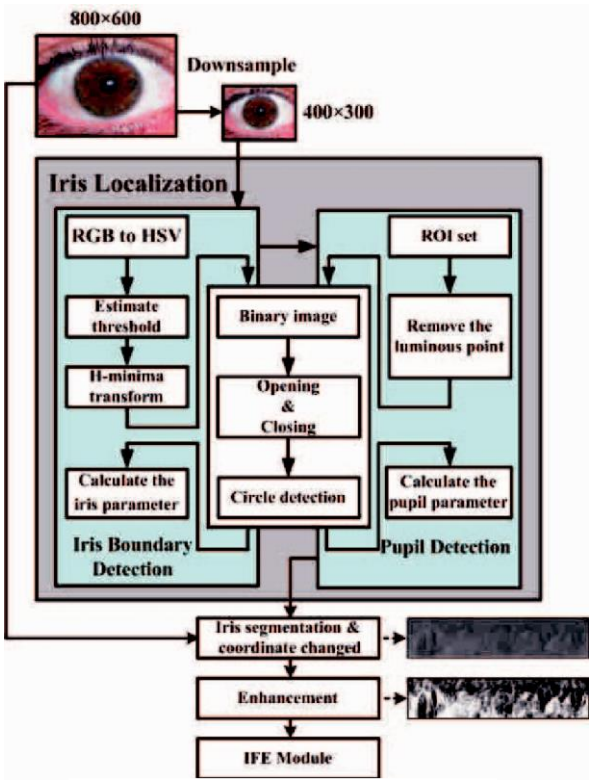


Fig. 4 Pre-processing module

3*) Iris Segmentation and Coordinate Transform Unit*

The localized iris image is transformed into polar coordinate system. When acquiring the human eye image,eyelids and eyelashes generally obscure the upper limbus of an iris, so we have to remove it. Finally it generates a rectangular iris image of a fixed size by linear interpolation. The image size of iris is 512□128[5].

4) Enhancement Unit

The normalized iris has low contrast. The final step is to perform image enhancement in order to obtain a good-quality image. It uses histogram equalization for the normalized iris image.

F. Finger Vein Recognition

Finger-vein matching is more stable, as compared with that of the texture.

1. Finger-Vein Image Pre-processing

The acquired finger images are noisy. Therefore, the acquired images are first subjected to pre-processing step that include: 1) Segmentation of ROI, 2) Translation and orientation alignment, and 3) Image enhancement to excerpt stable/reliable vascular patterns [12]. Finger-vein images are binarized, using a fixed threshold value as 230. The isolated and loosely connected regions in the binarized images are eliminated in two steps: First, the Sobel edge detector is used to eliminate number of connected white pixels being less than a threshold. Finally we got ROI image. Fig. 5 shows image samples from preprocessing steps that automatically ensures reliable segmentation of ROI.

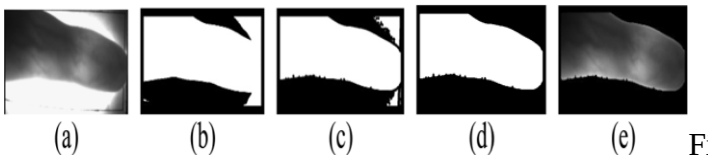


Fig. 5. Extraction of ROI from finger vein images. (a) Acquired image sample.(b) Binarized image. (c) Edge map subtracted from (b). (d) ROI mask from the image in (c) and the ROI finger vein image.(e) ROI image.

2. Finger-Vein Feature Extraction

In this paper, we propose finger-vein feature extraction using Gabor filters. It's also to enhance the extracted vein structures.

Gabor Filters for Feature Extraction: The analytical form of 2-D Gabor filters can be expressed as

$$h(\boldsymbol{p})_\theta = \frac{1}{2\pi|C|^{\frac{1}{2}}} \cos \boldsymbol{\omega}_m^T(\boldsymbol{p}_n - \boldsymbol{p}_0) \times \exp\left[-\frac{1}{2}(\boldsymbol{p}_n - \boldsymbol{p}_0)^T C^{-1}(\boldsymbol{p}_n - \boldsymbol{p}_0)\right]^T \quad (8)$$

3. Generating Finger-Vein Matching Scores

The matching scores between two finger-vein features are generated as follows:

$$s_v(R,T) = \min_{\forall i \in [0,2w], \forall j \in [0,2h]} \times \left(\frac{\sum_{x=1}^{m}\sum_{y=1}^{n} \odot \left(\hat{\boldsymbol{R}}(x+i, y+j), \boldsymbol{T}(x,y)\right)}{\sum_{x=1}^{m}\sum_{y=1}^{n}\left(\hat{\boldsymbol{R}}(x+i, y+j) \oplus -1\right)} \right) \quad (9)$$

By using this equation, we can decide whether the person is genuine or not.

V. CONCLUSION

In this paper, we propose an efficient way for human authentication using FKP, FV and Iris images. In the proposed technique, we have applied LDA pre-processed FKP image. In IRIS proposed technique, we have enforced is Gabor Wavelet transform on the pre-processed IRIS image. In Finger vein the repeated line tracking method gives a correct result in finger-vein identification: It repeatedly traces the vein in horizontal and vertical orientations and the starting seed is randomly selected; the whole process is repeatedly done for a particular amount of times. The acceptance rate is then computed. If the acceptance rate is greater than 80%, the person can be accepted. Otherwise, they will be rejected [11].

The Euclidean distance is used for the information fusion of different biometrics at feature level is able to increase the recognition rates to a higher value. In this case, the recognition rate obtained by fusion of multiple biometrics at feature level is 97.96%. We believe that the recognition rate can be improved.

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